WINSOURCE ELECTRONICS

THE DATASHEET OF

LM317LIPK

LM317L 3-Terminal Adjustable Regulator

1 Features

- Output Voltage Range Adjustable 1.25 V to 32 V When Used With External Resistor Divider
- Output Current Capability of 100 mA
- Input Regulation Typically 0.01% Per Input-Voltage Change
- Output Regulation Typically 0.5%
- Ripple Rejection Typically 80 dB
- For Higher Output Current Requirements, See LM317M (500 mA) and LM317 (1.5 A)

2 Applications

- Electronic Points of Sale
- Medical, Health, and Fitness Applications
- Printers
- Appliances and White Goods
- TV Set-Top Boxes

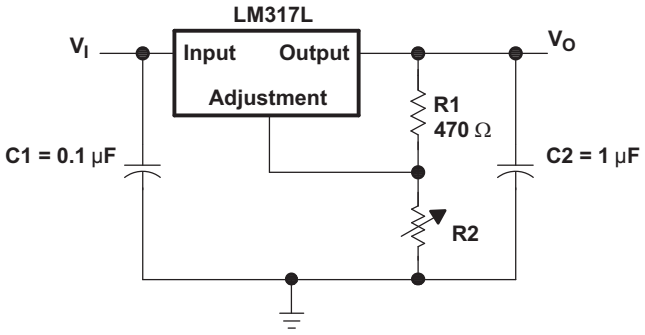
3 Description

The LM317L device is an adjustable, 3-terminal, positive-voltage regulator capable of supplying 100 mA over an output-voltage range of 1.25 V to 32 V. It is exceptionally easy to use and requires only two external resistors to set the output voltage.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM317L	SOIC (8)	4.90 mm × 3.91 mm
	TO-92 (3)	4.30 mm × 4.30 mm
	SOT-89 (3)	4.50 mm × 2.50 mm
	TSSOP (8)	3.00 mm × 4.40 mm

4 Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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5 Revision History

Changes from Revision D (October 2011) to Revision E **Page**

- Added *Device Information* table, *Pin Functions* table, *Handling Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Detailed Description*, *Application and Implementation*, *Power Supply Recommendations, Layout, Device and Documentation Support,* and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Deleted *Ordering Information* table. ... 1

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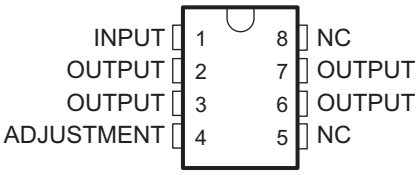
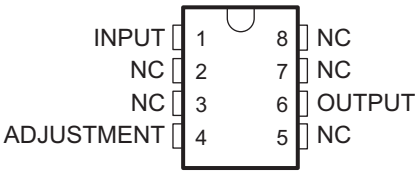
6 Pin Configuration and Functions

D PACKAGE
(TOP VIEW)



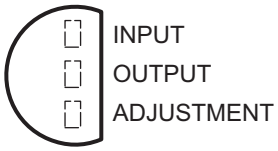
NC – No internal connection
OUTPUT terminals are all internally connected.

PW PACKAGE
(TOP VIEW)

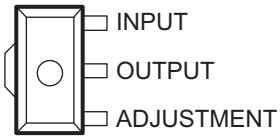


NC – No internal connection

LP PACKAGE
(TOP VIEW)



PK PACKAGE
(TOP VIEW)



Pin Functions

NAME	D, PW	LP, PK	TYPE	DESCRIPTION
ADJUSTMENT	4	√	I	Output feedback voltage
INPUT	1	√	I	Input supply voltage
NC	5	√	—	No connect
	8			
OUTPUT	2	√	O	Regulated output voltage
	3			
	6			
	7			

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7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_I - V_O$	Input-to-output differential voltage		35	V
T_J	Operating virtual-junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_O	Output voltage		1.25	32	V
$V_I - V_O$	Input-to-output voltage differential		2.5	32	V
I_O	Output current		2.5	100	mA
T_J	Operating virtual-junction temperature	LM317LC	0	125	°C
		LM317LI	–40	125	

7.4 Thermal Information

THERMAL METRIC(1)		LM317L				UNIT
		D 8 PINS	LP 3 PINS	PK 3 PINS	PW 8 PINS	
$R\theta_{JA}$	Junction-to-ambient thermal resistance	97.1	139.5	51.5	149.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

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7.5 Electrical Characteristics

over recommended operating virtual-junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
Input voltage regulation(2)	$V_I - V_O$ = 5 V to 35 V	T_J = 25°C		0.01	0.02	%V
		I_O = 2.5 mA to 100 mA		0.02	0.05	
Ripple regulation	V_O = 10 V,	f = 120 Hz		65		dB
	V_O = 10 V, 10-µF capacitor between ADJUSTMENT and ground		66	80		
Output voltage regulation	V_I = 5 V to 35 V, T_J = 25°C, I_O = 2.5 mA to 100 mA,	$V_O \le 5$ V		25		mV
		$V_O \ge 5$ V		5		mV/V
	V_I = 5 V to 35 V, I_O = 2.5 mA to 100 mA	$V_O \le 5$ V		50		mV
		$V_O \ge 5$ V		10		mV/V
Output voltage change with temperature	T_J = 0°C to 125°C			10		mV/V
Output voltage long-term drift	After 1000 hours at T_J = 125°C and $V_I - V_O$ = 35 V			3	10	mV/V
Output noise voltage	f = 10 Hz to 10 kHz,	T_J = 25°C		30		µV/V
Minimum output current to maintain regulation	$V_I - V_O$ = 35 V			1.5	2.5	mA
Peak output current	$V_I - V_O \le 35$ V		100	200		mA
ADJUSTMENT current				50	100	µA
Change in ADJUSTMENT current	$V_I - V_O$ = 2.5 V to 35 V,	I_O = 2.5 mA to 100 mA		0.2	5	µA
Reference voltage (output to ADJUSTMENT)	$V_I - V_O$ = 5 V to 35 V, P ≤ rated dissipation	I_O = 2.5 mA to 100 mA,	1.2	1.25	1.3	V

(1) Unless otherwise noted, these specifications apply for the following test conditions: $V_I - V_O$ = 5 V and I_O = 40 mA. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible. All characteristics are measured with a 0.1-µF capacitor across the input and a 1-µF capacitor across the output.
(2) Input voltage regulation is expressed here as the percentage change in output voltage per 1-V change at the input.

7.6 Typical Characteristics

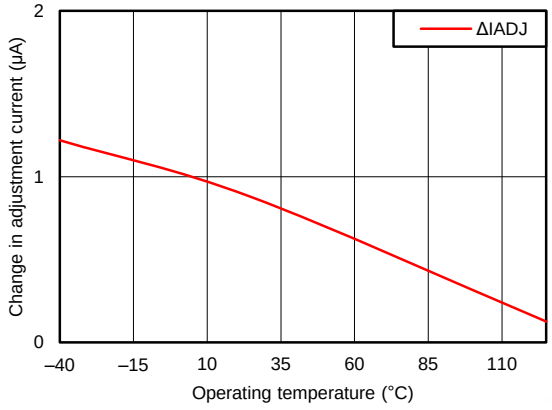


Figure 1. Change in Adjustment Current Over Temperature

8 Detailed Description

8.1 Overview

The LM317L device is a 100-mA linear regulator with high voltage tolerance up to 35 V. The device has a feedback voltage that is relative to the output instead of ground. This ungrounded design allows the LM317L device to have superior line and load regulation. This design also allows the LM317L device to be used as a current source or current sink using a single resistor. Any output voltage from 1.25 to 32 V can be obtained by using two resistors. The bias current of the device, up to 2.5 mA, flows to the output; this current must be used by the load or the feedback resistors. The power dissipation is the product of pass-element voltage and current, which is calculated as shown in Equation 1.

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (1)$$

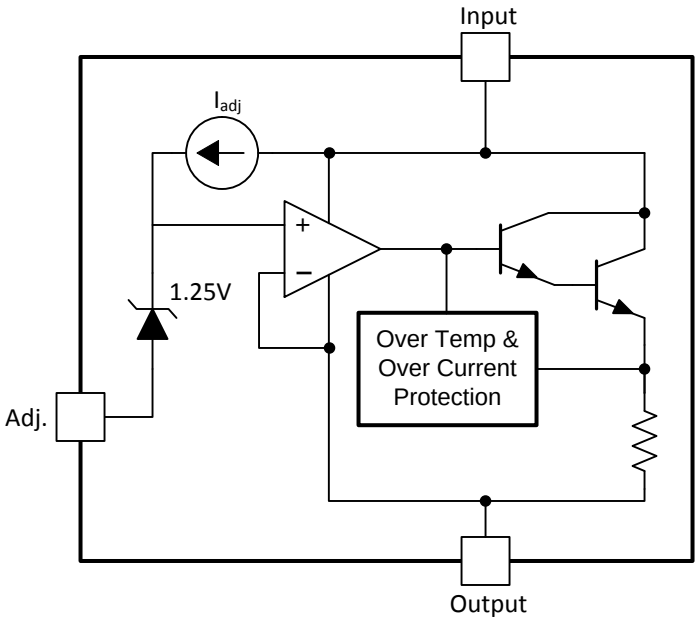
The application heat sink must be able to absorb the power calculated in Equation 1.

In addition to higher performance than fixed regulators, this regulator offers full overload protection, available only in integrated circuits. Included on the chip are current-limiting and thermal-overload protection. All overload-protection circuitry remains fully functional even when ADJUSTMENT is disconnected. Normally, no capacitors are needed unless the device is situated far from the input filter capacitors, in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. ADJUSTMENT can be bypassed to achieve very high ripple rejection, which is difficult to achieve with standard three-terminal regulators.

In addition to replacing fixed regulators, the LM317L regulator is useful in a wide variety of other applications. Since the regulator is floating and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded. Its primary application is that of a programmable output regulator, but by connecting a fixed resistor between ADJUSTMENT and OUTPUT, this device can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping ADJUSTMENT to ground, programming the output to 1.25 V, where most loads draw little current.

The LM317LC device is characterized for operation over the virtual junction temperature range of 0°C to 125°C. The LM317LI device is characterized for operation over the virtual junction temperature range of –40°C to 125°C.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 NPN Darlington Output Drive

NPN Darlington output topology provides naturally low output impedance and an output capacitor is optional. To support maximum current and lowest temperature, 2.5-V headroom is recommended ($V_I – V_O$).

8.3.2 Overload Block

Over-current and over-temperature shutdown protects the device against overload or damage from operating in excessive heat.

8.3.3 Programmable Feedback

Op amp with 1.25-V offset input at the ADJUST pin provides easy output voltage or current (not both) programming. For current regulation applications, a single resistor whose resistance value is 1.25 V / I_{OUT} and power rating is greater than $(1.25\ V)^2$ / R should be used. For voltage regulation applications, two resistors set the output voltage. See *Typical Application* for a schematic and the resistor formula.

8.4 Device Functional Modes

8.4.1 Normal operation

The device OUTPUT pin will source current necessary to make OUTPUT pin 1.25 V greater than ADJUST terminal to provide output regulation.

8.4.2 Operation With Low Input Voltage

The device requires up to 2.5-V headroom ($V_I – V_O$) to operate in regulation. With less headroom, the device may drop out and OUTPUT voltage will be INPUT voltage minus drop out voltage.

8.4.3 Operation at Light Loads

The device passes its bias current to the OUTPUT pin. The load or feedback must consume this minimum current for regulation or the output may be too high.

8.4.4 Operation In Self Protection

When an overload occurs the device will shut down Darlington NPN output stage or reduce the output current to prevent device damage. The device will automatically reset from the overload. The output may be reduced or alternate between on and off until the overload is removed.

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9 Application and Implementation

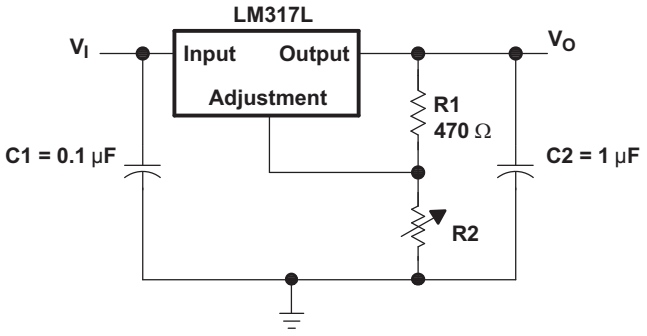
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The two output resistors are the only components required to adjust V_{OUT}.

9.2 Typical Application



9.2.1 Design Requirements

1. Use of an input bypass capacitor is recommended if regulator is far from the filter capacitors.
2. For this design example, use the parameters listed in Table 1.
3. Use of an output capacitor improves transient response, but is optional.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	(Output Voltage + 2.5 V) to 32 V
Output voltage	$V_{REF} \times (1 + R_2 / R_1) + I_{ADJ} \times R_2$

9.2.2 Detailed Design Procedure

9.2.2.1 Input Capacitor

An input capacitor is not required, but it is recommended, particularly if the regulator is not in close proximity to the power-supply filter capacitors. A 0.1-µF ceramic or 1-µF tantalum provides sufficient bypassing for most applications, especially when adjustment and output capacitors are used.

9.2.2.2 Output Capacitor

An output capacitor improves transient response, but it not needed for stability.

9.2.2.3 Feedback Resistors

The feedback resistor set the output voltage using Equation 2.

$$V_{REF} \times (1 + R_2 / R_1) + I_{ADJ} \times R_2 \quad (2)$$

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9.2.2.4 Adjustment Terminal Capacitor

The optional adjustment pin capacitor will improve ripple rejection by preventing the amplification of the ripple. When capacitor is used and V_{OUT} > 6 V, a protection diode from adjust to output is recommended.

9.2.2.5 Design Options and Parameters

Common Linear Regulator designs are concerned with the following parameters:

- Input voltage range
- Input capacitor range
- Output voltage
- Output current rating
- Output capacitor range
- Input short protection
- Stability
- Ripple rejection

9.2.2.6 Output Voltage

V_O is calculated as shown in Equation 3.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_2}{R_1}\right) + (I_{ADJ} \times R_2) \tag{3}$$

Because I_{ADJ} typically is 50 µA, it is negligible in most applications.

9.2.2.7 Ripple Rejection

C_{ADJ} is used to improve ripple rejection; it prevents amplification of the ripple as the output voltage is adjusted higher. If C_{ADJ} is used, it is best to include protection diodes.

9.2.2.8 Input Short Protection

If the input is shorted to ground during a fault condition, protection diodes provide measures to prevent the possibility of external capacitors discharging through low-impedance paths in the IC. By providing low-impedance discharge paths for C_O and C_{ADJ}, respectively, D1 and D2 prevent the capacitors from discharging into the output of the regulator.

9.2.3 Application Curves

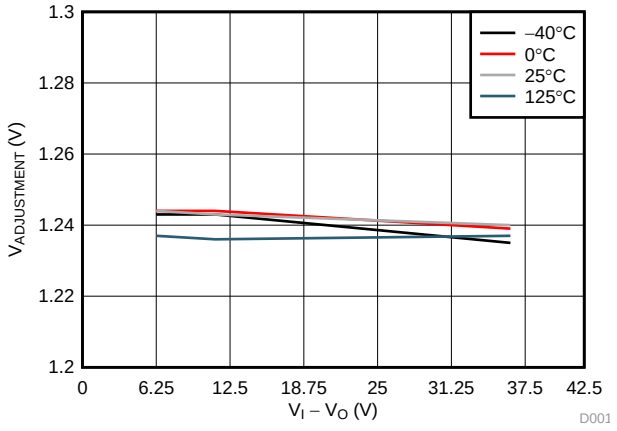

Figure 2. Adjustment Voltage Relative to Output Over Temperature

9.3 General Configurations

9.3.1 Regulator Circuit With Improved Ripple Rejection

C2 helps to stabilize the voltage at the adjustment pin, which will help reject noise. Diode D1 exists to discharge C2 in case the output is shorted to ground.

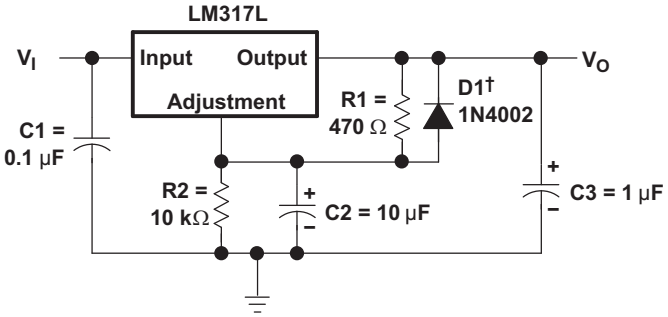

Figure 3. Regulator Circuit With Improved Ripple Rejection

9.3.2 0-V to 30-V Regulator Circuit

In the 0-V to 30-V regulator circuit application, the output voltage is determined by Equation 4.

$$V_{OUT} = V_{REF}\left(1 + \frac{R_2 + R_3}{R_1}\right) - 10\,V \tag{4}$$

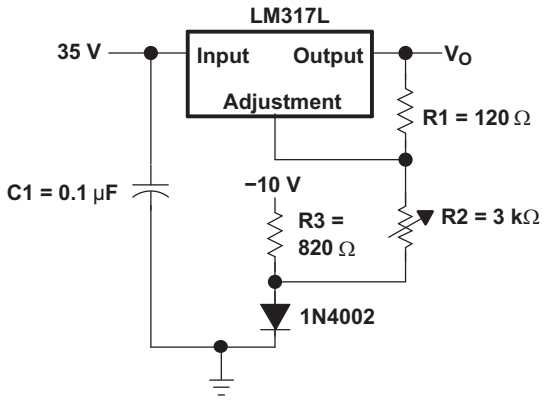

Figure 4. 0-V to 30-V Regulator Circuit

9.3.3 Precision Current-Limiter Circuit

This application will limit the output current to the I_{LIMIT} shown in Figure 5.

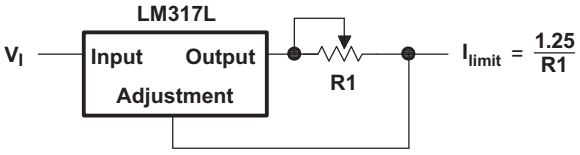

Figure 5. Precision Current-Limiter Circuit

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General Configurations (continued)

9.3.4 Tracking Preregulator Circuit

The tracking preregulator circuit application keeps a constant voltage across the second LM317L in the circuit.

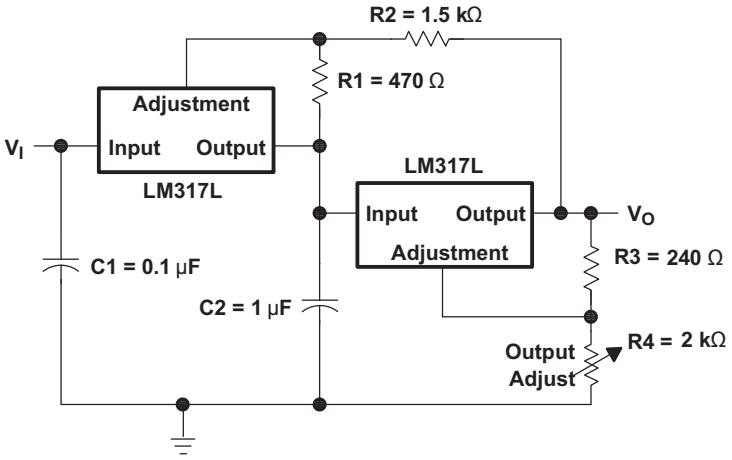

Figure 6. Tracking Preregulator Circuit

9.3.5 Slow-Turn On 15-V Regulator Circuit

The capacitor C1, in combination with the PNP transistor, helps the circuit to slowly start supplying voltage. In the beginning, the capacitor is not charged. Therefore, output voltage will start at 1.9 V, as determined by Equation 5. As the capacitor voltage rises, V_{OUT} will rise at the same rate. When the output voltage reaches the value determined by R1 and R2, the PNP will be turned off.

$$V_{C1} + V_{BE} + 1.25\ V = 0\ V + 0.65\ V + 1.25\ V = 1.9\ V \quad (5)$$

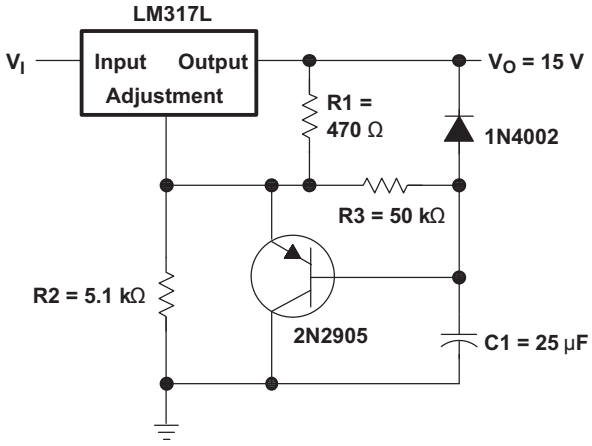

Figure 7. Slow-Turn On 15-V Regulator Circuit

General Configurations (continued)

9.3.6 50-mA Constant-Current Battery-Charger Circuit

The current-limit operation mode can be used to trickle charge a battery at a fixed current as determined by Equation 6. V_I should be greater than V_{BAT} + 3.75 V.

$$I_{CHG} = 1.25\ V \div 24\ \Omega \quad (6)$$

(1.25 V [V_{REF}] + 2.5 V [headroom]) (7)

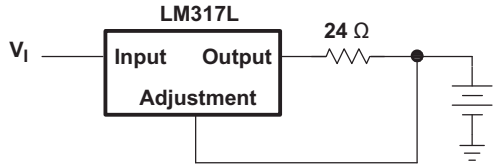

Figure 8. 50-mA Constant-Current Battery-Charger Circuit

9.3.7 Current-Limited 6-V Charger

As the charge current increases, the voltage at the bottom resistor increases until the NPN starts sinking current from the adjustment pin. The voltage at the adjustment pin will drop, and consequently the output voltage will decrease until the NPN stops conducting.

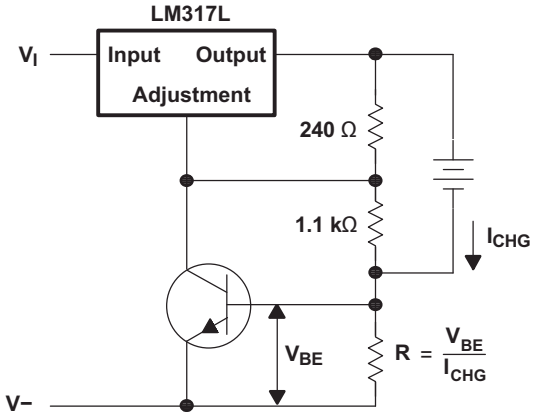

Figure 9. Current-Limited 6-V Charger

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General Configurations (continued)

9.3.8 High-Current Adjustable Regulator

This application allows higher currents at V_{OUT} than the LM317L device can provide, while still keeping the output voltage at levels determined by the adjustment-pin resistor divider of the LM317L.

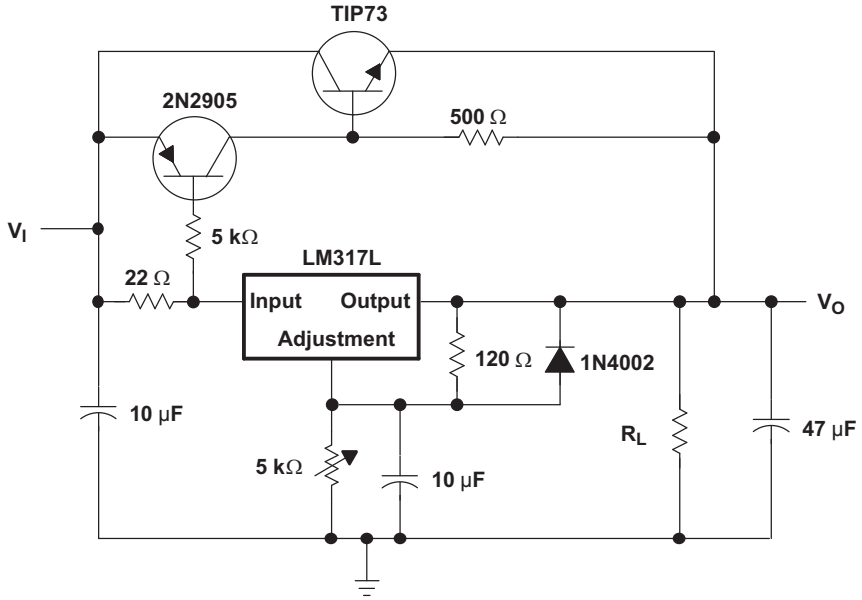

Figure 10. High-Current Adjustable Regulator

10 Power Supply Recommendations

The LM317L device is designed to operate from an input voltage supply range between 2.5 V to 32 V greater than the output voltage. If the device is more than six inches from the input filter capacitors, an input bypass capacitor, 0.1 µF or greater, of any type is needed for stability.

11 Layout

11.1 Layout Guidelines

- It is recommended that the input pin be bypassed to ground with a bypass-capacitor.
- The optimum placement is closest to the VIN of the device and GND of the system. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the VIN pin, and the GND pin of the system.
- For operation at full-rated load, it is recommended to use wide trace lengths to eliminate IR drop and heat dissipation.

11.2 Layout Example

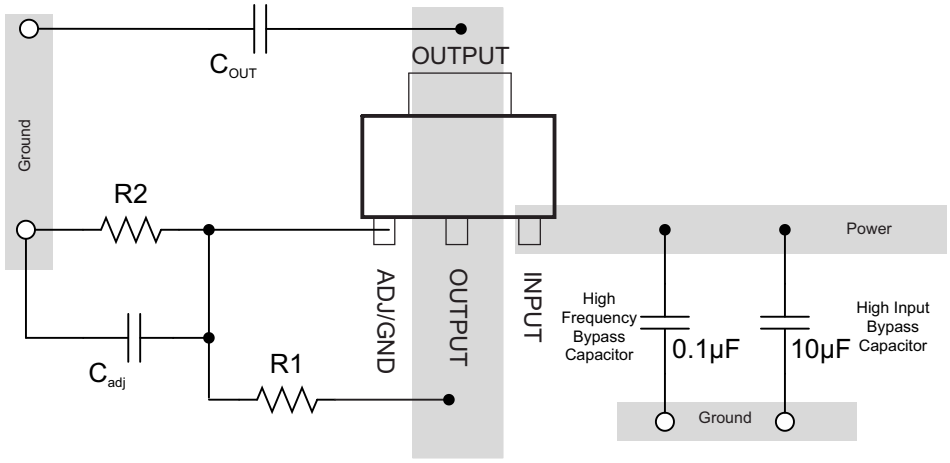

Figure 11. Layout Diagram

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12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM317LCD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC	Samples
LM317LCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 125	L317LC	Samples
LM317LCDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC	Samples
LM317LCLP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	L317LC	Samples
LM317LCLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	L317LC	Samples
LM317LCLPRE3	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	L317LC	Samples
LM317LCPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	LA	Samples
LM317LCPKG3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	LA	Samples
LM317LCPW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC	Samples
LM317LCPWE4	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC	Samples
LM317LCPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC	Samples
LM317LCPWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC	Samples
LM317LID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L317LI	Samples
LM317LIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L317LI	Samples
LM317LIDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L317LI	Samples
LM317LILP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	L317LI	Samples
LM317LILPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	L317LI	Samples
LM317LIPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	LB	Samples
LM317LIPKG3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	LB	Samples
LM317LIPW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L317LI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM317LIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L317LI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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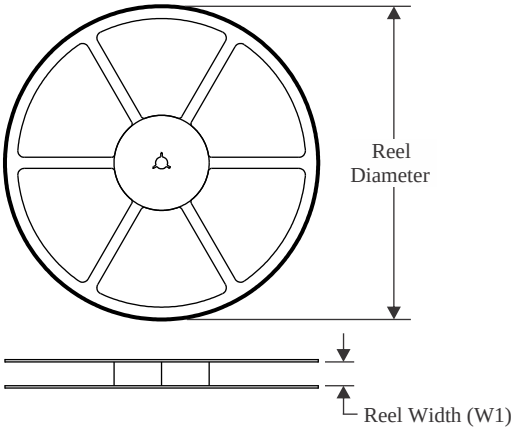
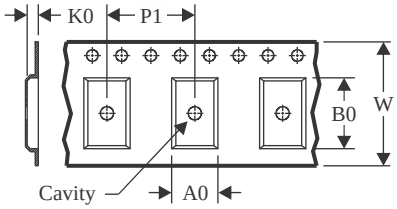
TAPE AND REEL INFORMATION

REEL DIMENSIONS

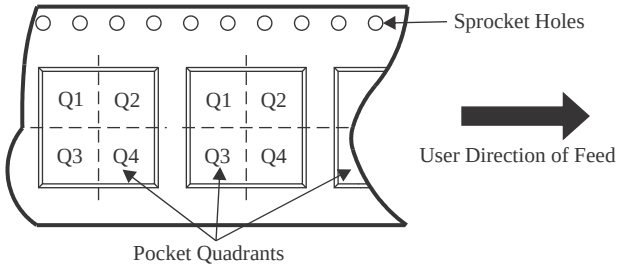


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

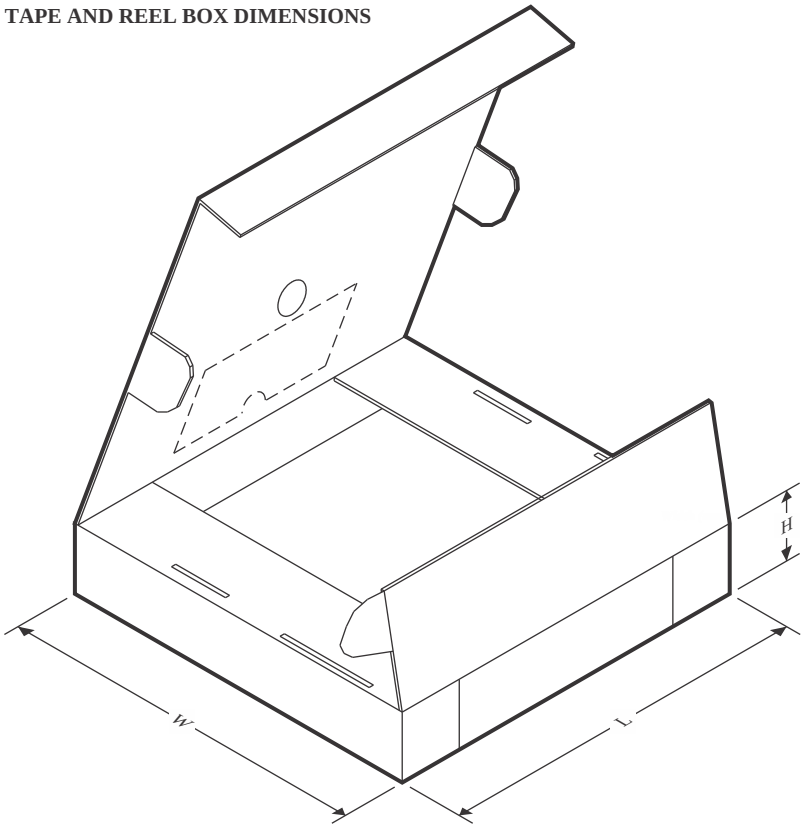
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM317LCDR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM317LCDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM317LCPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
LM317LCPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM317LIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM317LIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM317LIPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
LM317LIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

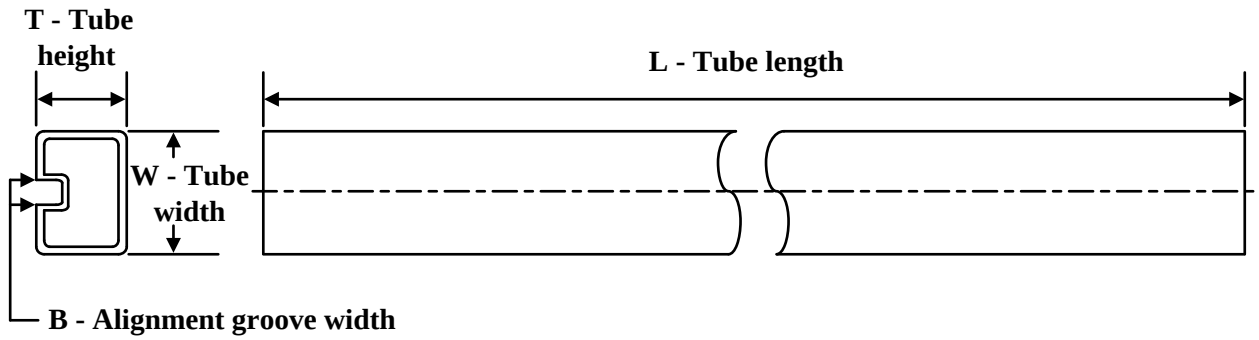
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM317LCDR	SOIC	D	8	2500	364.0	364.0	27.0
LM317LCDRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM317LCPK	SOT-89	PK	3	1000	340.0	340.0	38.0
LM317LCPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LM317LIDR	SOIC	D	8	2500	340.5	338.1	20.6
LM317LIDRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM317LIPK	SOT-89	PK	3	1000	340.0	340.0	38.0
LM317LIPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

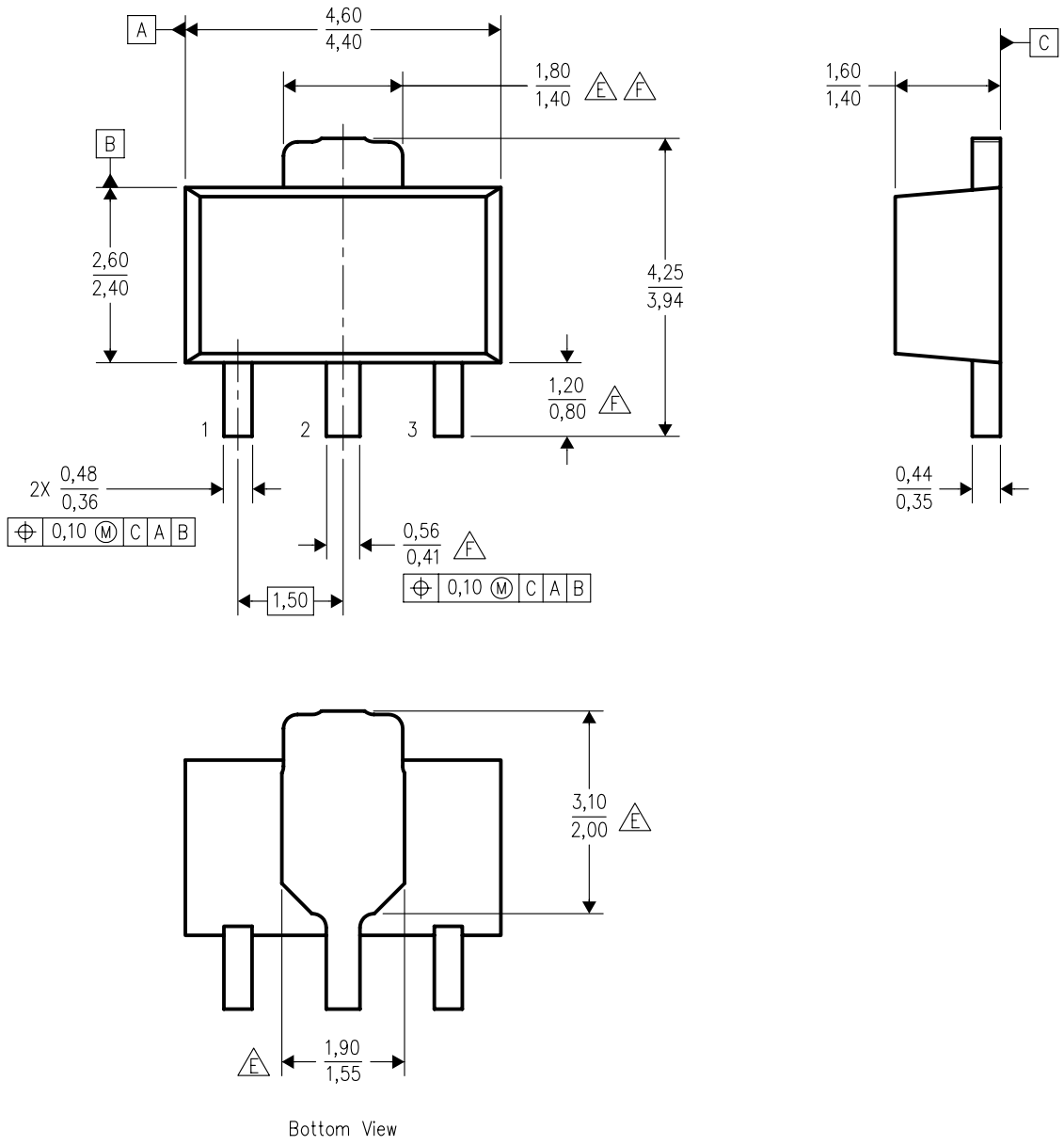
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM317LCD	D	SOIC	8	75	507	8	3940	4.32
LM317LCPW	PW	TSSOP	8	150	530	10.2	3600	3.5
LM317LCPWE4	PW	TSSOP	8	150	530	10.2	3600	3.5
LM317LID	D	SOIC	8	75	507	8	3940	4.32
LM317LIPW	PW	TSSOP	8	150	530	10.2	3600	3.5

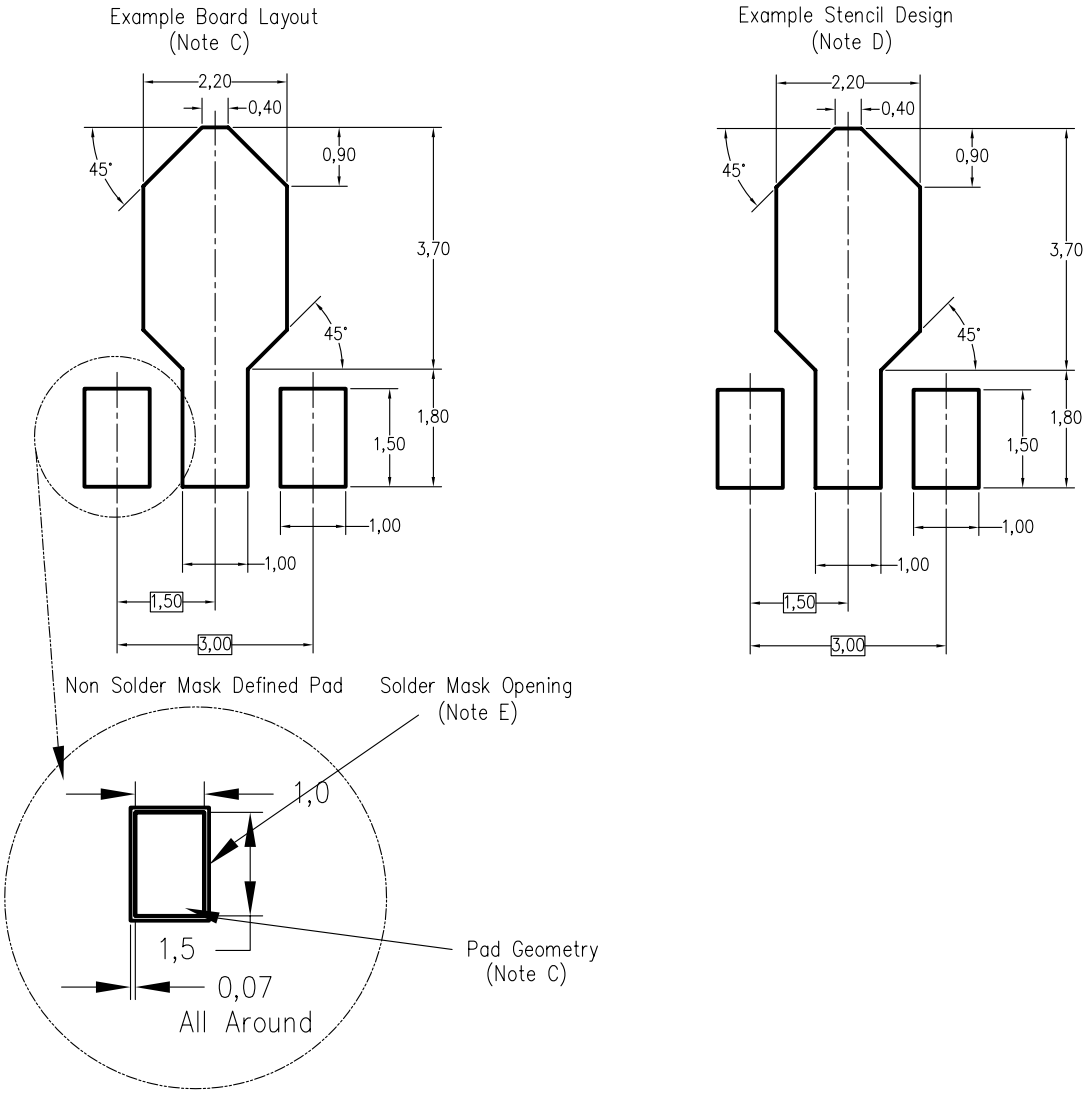
PK (R–PSSO–F3) PLASTIC SINGLE–IN–LINE PACKAGE



4040234/D 02/2006

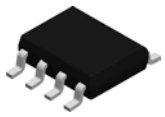
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the tab.
D. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.15 per side.
E. Thermal pad contour optional within these dimensions.
F. Falls within JEDEC TO–243 variation AA, except minimum lead length, pin 2 minimum lead width, minimum tab width.

PK (R–PDSO–G3)



4208221/A 09/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

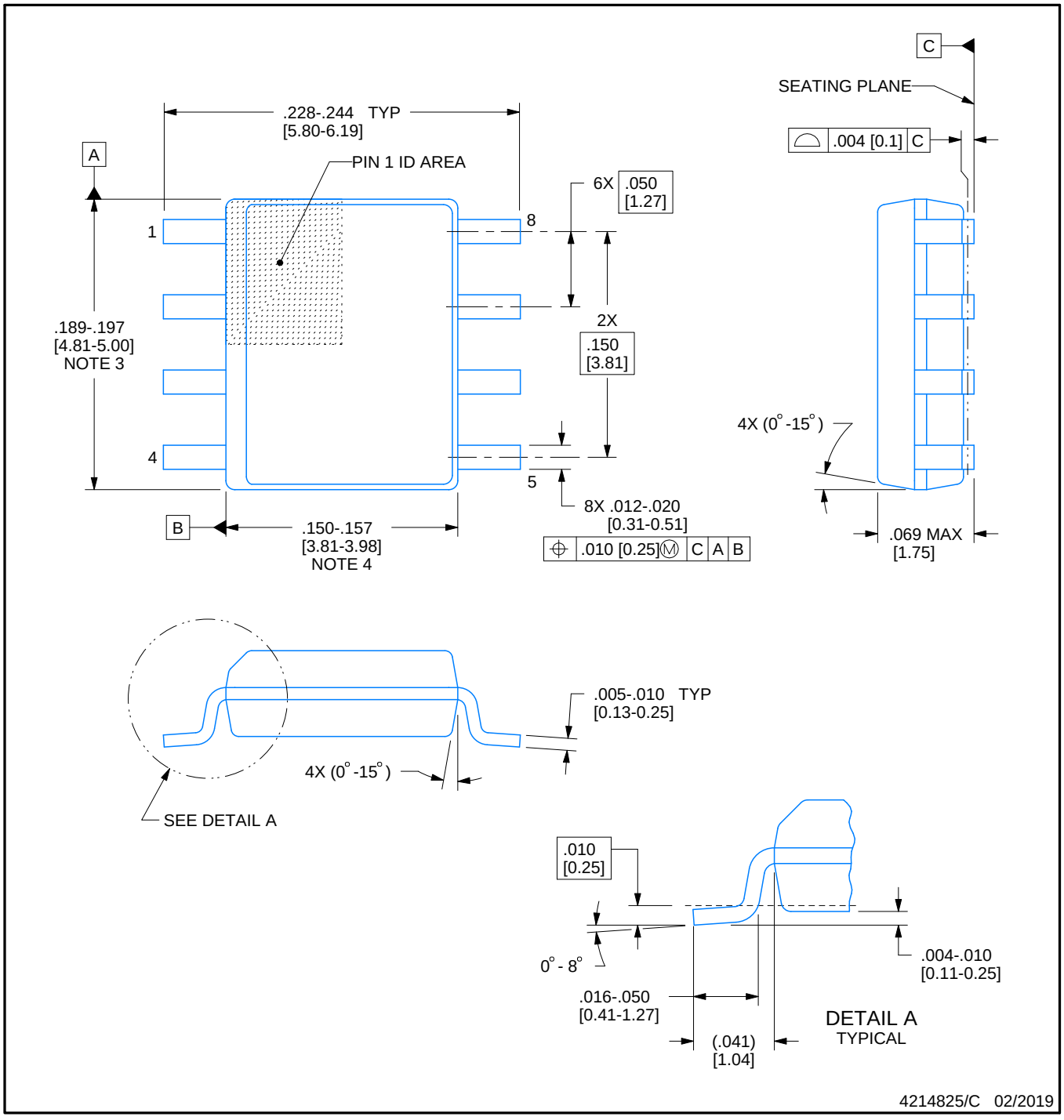


PACKAGE OUTLINE

D0008A

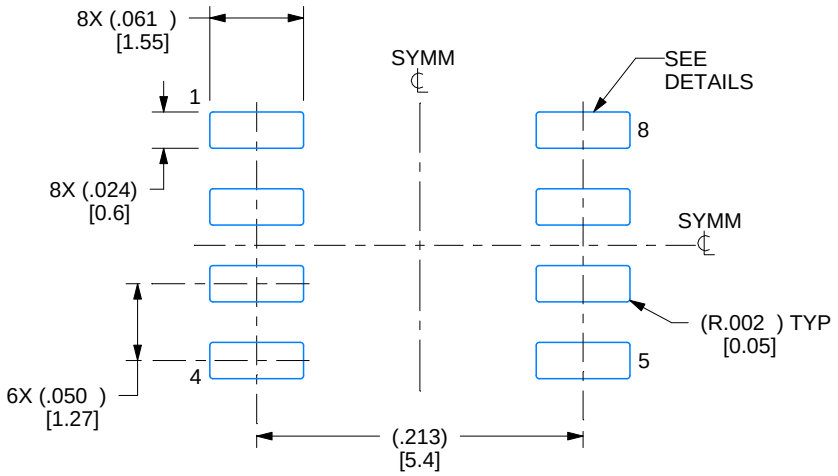
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

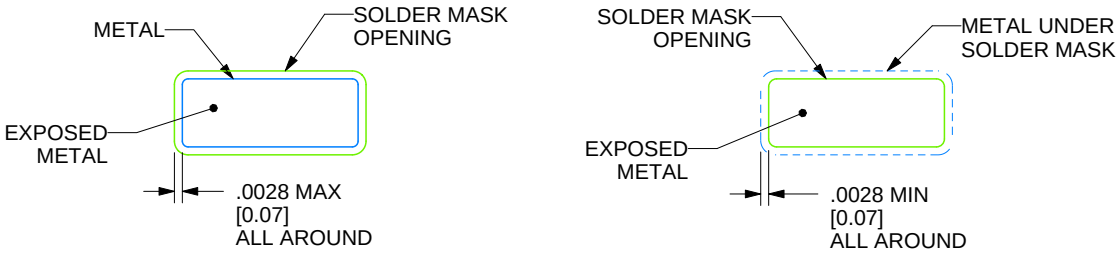


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

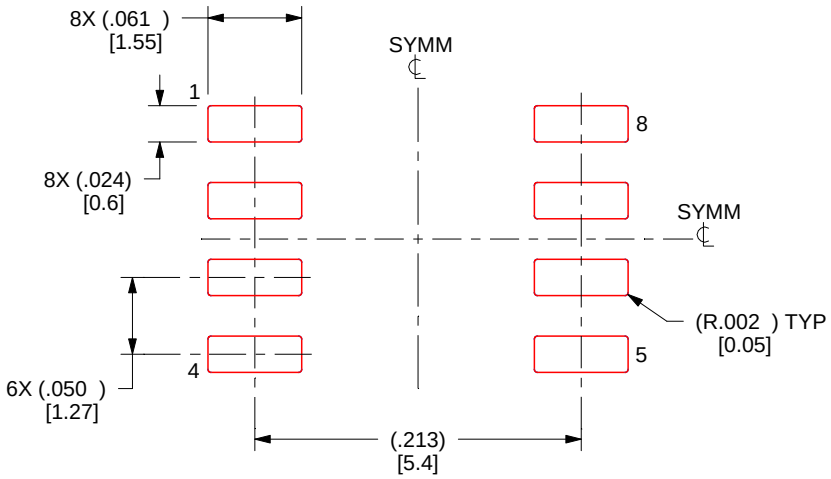
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

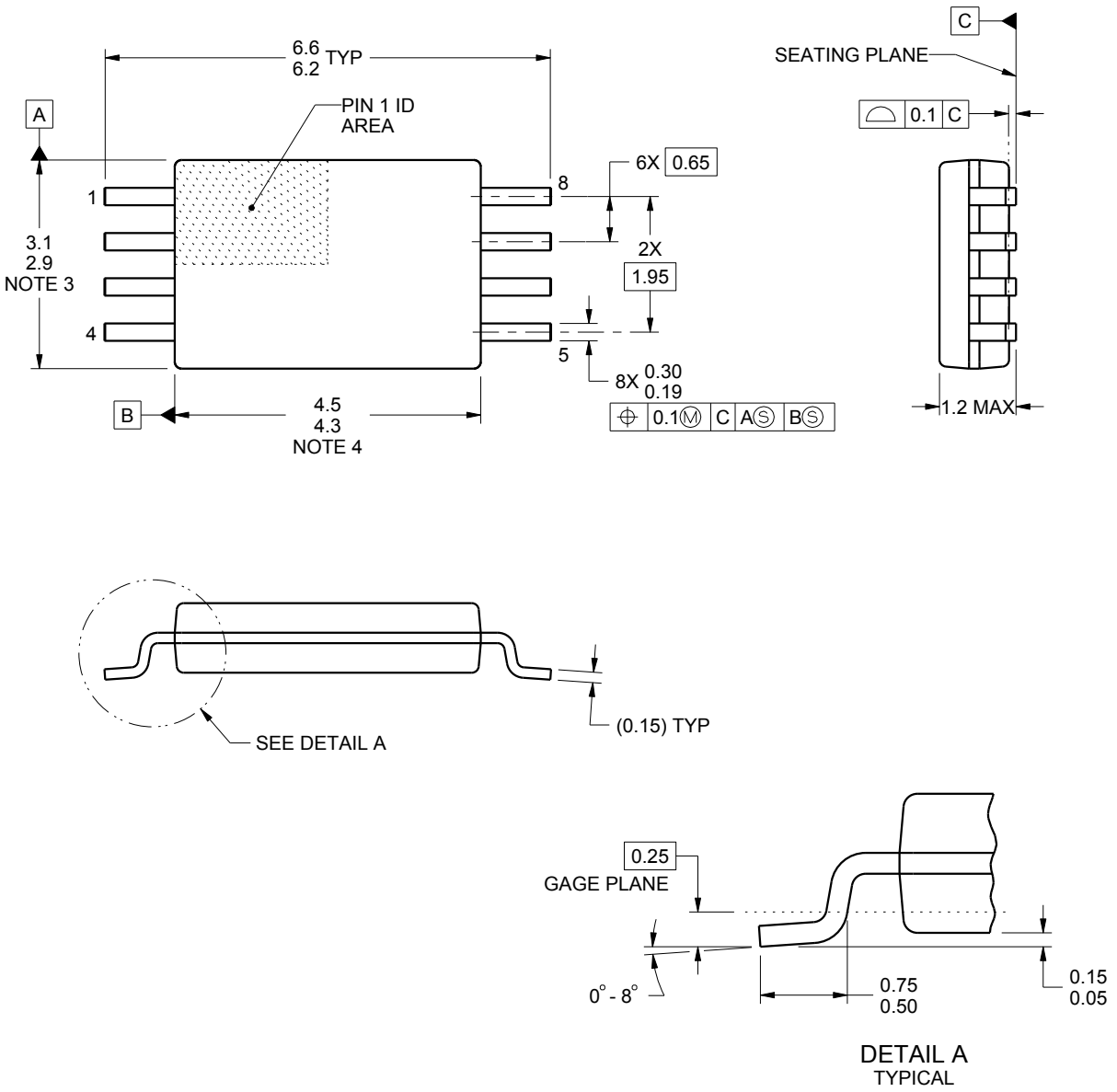
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

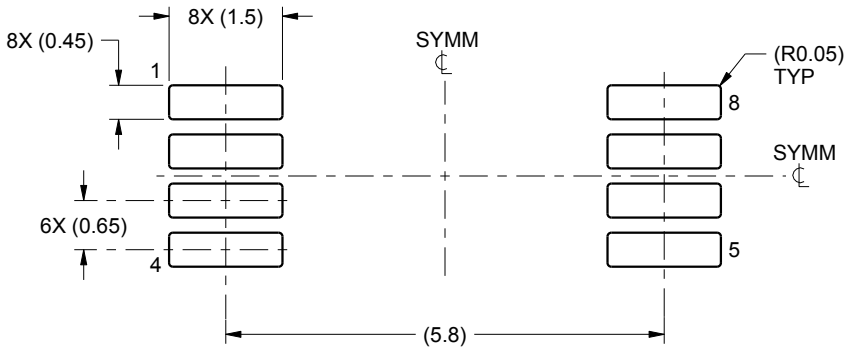
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

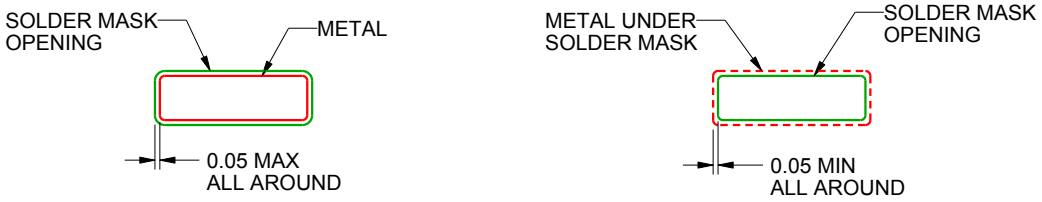


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

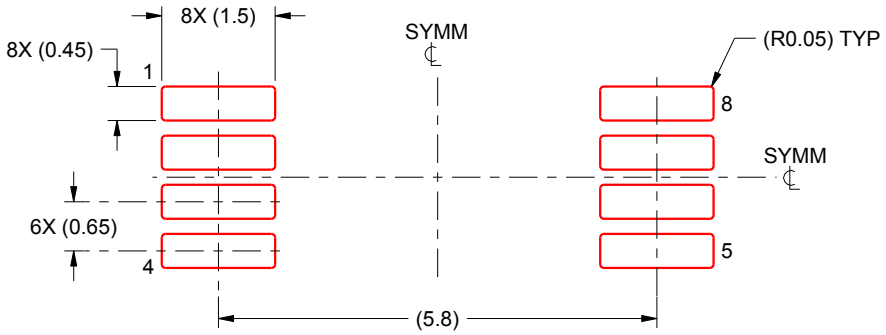


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

LP 3 TO-92 - 5.34 mm max height

TRANSISTOR OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

LP0003A

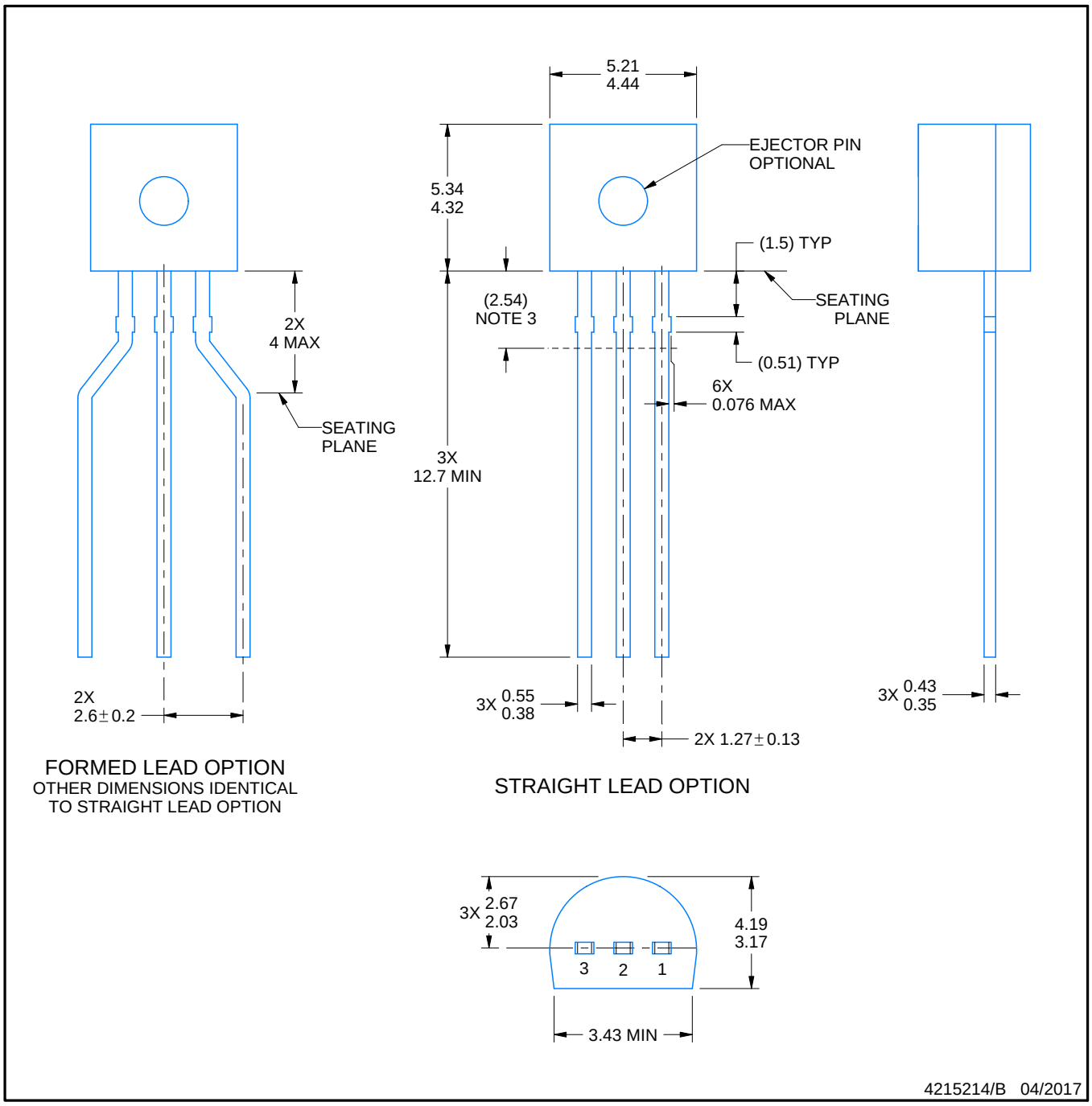




PACKAGE OUTLINE

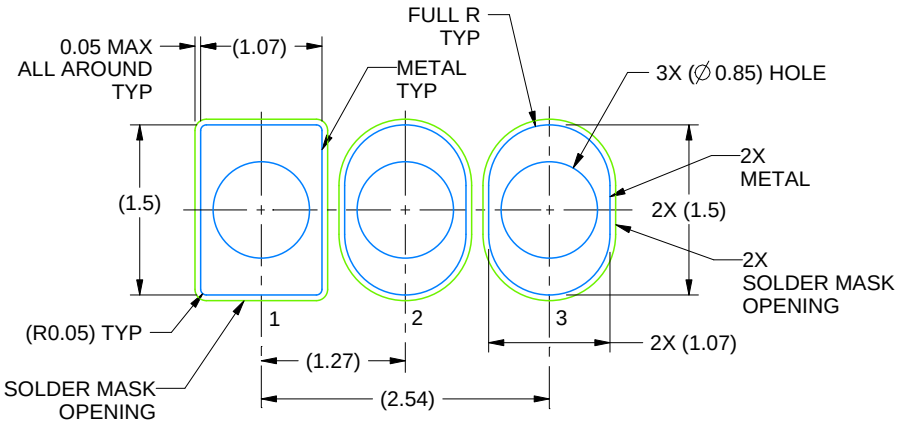
TO-92 - 5.34 mm max height

TO-92

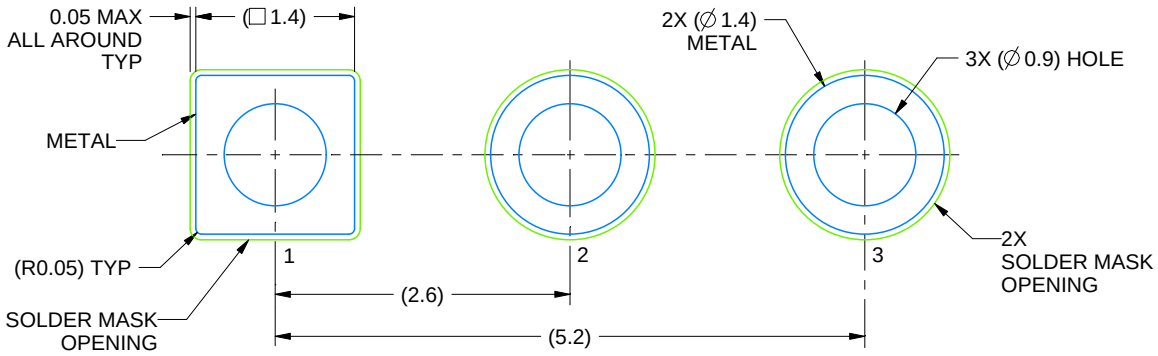


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



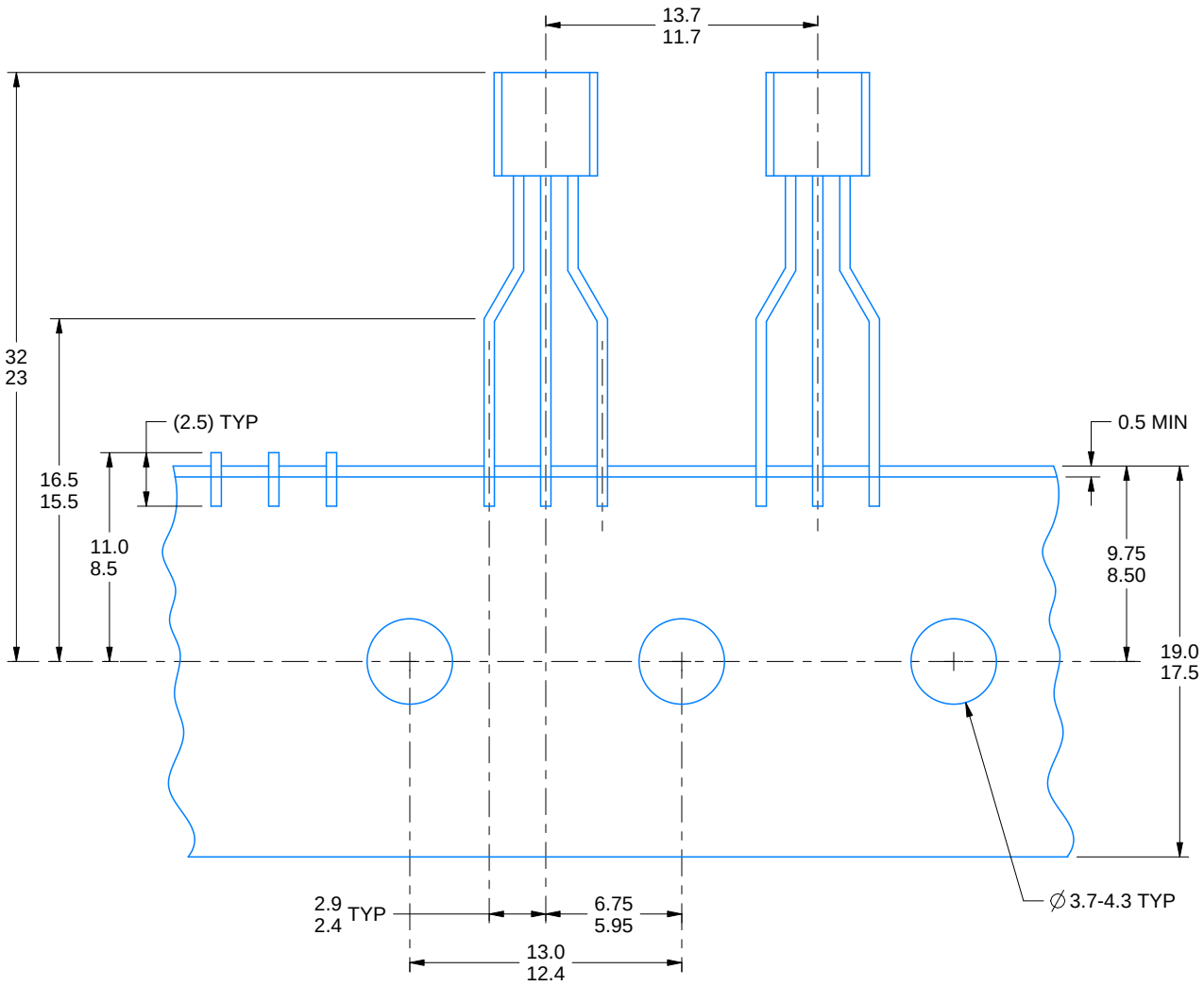
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/B 04/2017

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

4215214/B 04/2017

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