



**THE DATASHEET OF  
PE42424A-Z**



# PE42424

UltraCMOS® SPDT RF Switch  
100 MHz–6 GHz

### Product Description

The PE42424 is a HaRP™ technology-enhanced reflective 50Ω SPDT RF switch designed for use in high power and high performance WLAN 802.11 a/b/g/n/ac applications such as carrier and enterprise Wi-Fi products supporting bandwidths up to 6 GHz.

This switch features exceptional port-to-port isolation, fast switching speed, and high power handling, all in a compact 1.5 × 1.5 mm package. PE42424 also features high linearity that remains invariant over the full power supply range. In addition, this device has robust ESD and temperature performance and does not require blocking capacitors or any external matching components.

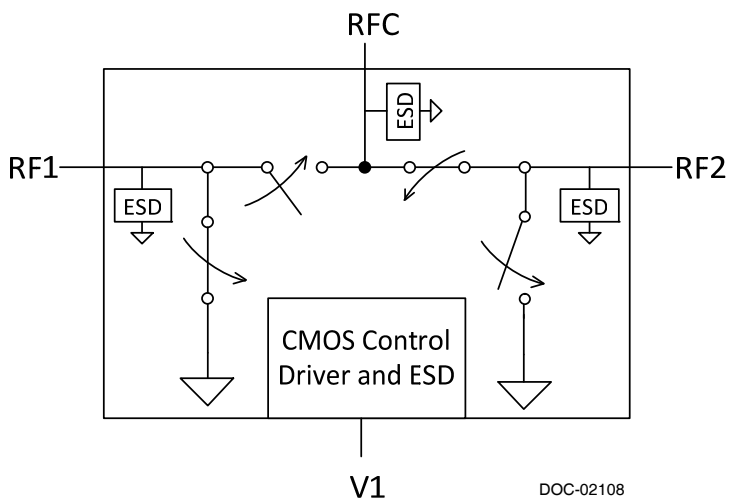
The PE42424 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

Peregrine's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

### Features

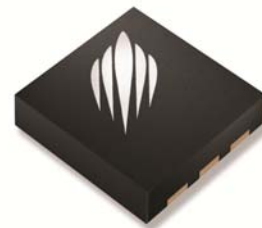
- 802.11 a/b/g/n/ac support
- Exceptional isolation
  - 48 dB @ 2.4 GHz
  - 35 dB @ 5.8 GHz
- Fast switching
  - 145 ns switching time
  - 125 kHz switching rate
- High power handling
  - 39 dBm Pulsed
  - 30 dBm CW
- High linearity across supply range
  - IIP3 of 61 dBm
  - IIP2 of 125 dBm
- 1.8V control logic compatible
- 105 °C operating temperature
- ESD performance
  - 2500V HBM on RF pins to GND
  - 1000V CDM on all pins

**Figure 1. Functional Diagram**



**Figure 2. Package Type**

6-lead 1.5 × 1.5 mm DFN



**Table 1. Electrical Specifications @ 25°C, V<sub>DD</sub> = 3.3V, (Z<sub>L</sub> = Z<sub>S</sub> = 50Ω) unless otherwise specified**

| Parameter                                | Path    | Condition                             | Min | Typ  | Max  | Unit |
|--|---------|---------------------------------------|-----|------|------|------|
| Operating frequency                      |         |                                       | 100 |      | 6000 | MHz  |
| Insertion loss                           | RFC–RFX | 100–2500 MHz                          |     | 0.80 | 0.95 | dB   |
|  |         | 2500–5825 MHz                         |     | 0.90 | 1.15 | dB   |
|  |         | 5825–6000 MHz                         |     | 0.95 | 1.20 | dB   |
| Isolation                                | RFC–RFX | 100–2500 MHz                          | 45  | 47   |      | dB   |
|  |         | 2500–5825 MHz                         | 33  | 35   |      | dB   |
|  |         | 5825–6000 MHz                         | 33  | 34   |      | dB   |
| Isolation                                | RFX–RFX | 100–2500 MHz                          | 37  | 39   |      | dB   |
|  |         | 2500–5825 MHz                         | 29  | 30   |      | dB   |
|  |         | 5825–6000 MHz                         | 29  | 30   |      | dB   |
| Return loss<br>(common and active port)  | RFX     | 100–6000 MHz                          |     | 21   |      | dB   |
| Input 1dB compression point <sup>1</sup> | RFC–RFX | 6000 MHz                              |     | 41   |      | dBm  |
| Input IP3 <sup>2</sup>                   | RFC–RFX | 1900 MHz                              |     | 61   |      | dBm  |
| Input IP2 <sup>2</sup>                   | RFC–RFX | 1900 MHz                              |     | 125  |      | dBm  |
| 3rd harmonic                             | RFC–RFX | P <sub>IN</sub> = +30 dBm @ 1900 MHz  |     | 74   |      | dBc  |
| 2nd harmonic                             | RFC–RFX | P <sub>IN</sub> = +30 dBm @ 1900 MHz  |     | 85   |      | dBc  |
| Switching time                           |         | 50% CTRL to 90% or 10% of final value |     | 145  | 230  | ns   |

Notes: 1. The input 1dB compression point is a linearity figure of merit. Refer to *Table 3* for the operating RF input power (50Ω).  
2. The input intercept point remains invariant over the full supply range as defined in *Table 3*.

Figure 3. Pin Configuration (Top View)

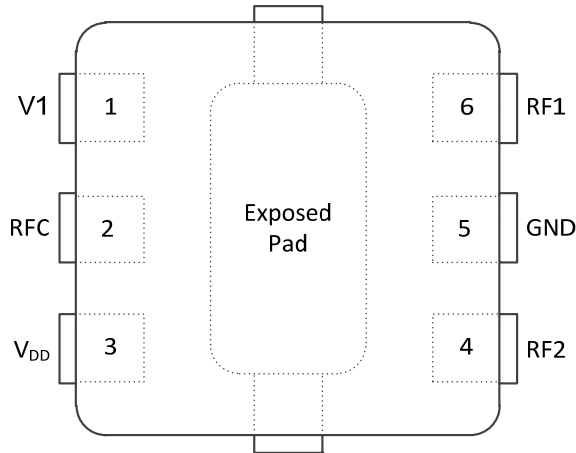


Table 2. Pin Descriptions

| Pin # | Pin Name        | Description                              |
|-------|-----------------|--|
| 1     | V1              | Digital control logic input 1            |
| 2     | RFC*            | RF common                                |
| 3     | V <sub>DD</sub> | Supply voltage (nominal 3.3V)            |
| 4     | RF2*            | RF port 2                                |
| 5     | GND             | Ground                                   |
| 6     | RF1*            | RF port 1                                |
| Pad   | GND             | Exposed pad: ground for proper operation |

Note: \* RF pins 2, 4 and 6 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.

Table 3. Operating Ranges

| Parameter                           | Symbol                  | Min  | Typ                                  | Max        | Unit     |
|-------------------------------------|-------------------------|------|--------------------------------------|------------|----------|
| Supply voltage                      | V <sub>DD</sub>         | 2.3  | 3.3                                  | 5.5        | V        |
| Supply current                      | I <sub>DD</sub>         |      | 130 <sup>1</sup><br>200 <sup>2</sup> | 200<br>300 | μA<br>μA |
| Digital input high (V1)             | V <sub>IH</sub>         | 1.4  |                                      | 3.6        | V        |
| Digital input low (V1)              | V <sub>IL</sub>         | -0.3 |                                      | 0.6        | V        |
| RF input power, CW                  | P <sub>MAX,CW</sub>     |      |                                      | 30         | dBm      |
| RF input power, pulsed <sup>3</sup> | P <sub>MAX,PULSED</sub> |      |                                      | 39         | dBm      |
| Operating temperature range         | T <sub>OP</sub>         | -40  | +25                                  | +105       | °C       |

Notes: 1. V<sub>IH</sub> > 1.7V  
2. 1.4V < V<sub>IH</sub> < 1.7V  
3. Pulsed, 5% duty cycle of 4620 μs period, 50Ω

Table 4. Absolute Maximum Ratings

| Parameter/Condition  | Symbol               | Min  | Max          | Unit   |
|--|----------------------|------|--------------|--------|
| Supply voltage   | V <sub>DD</sub>      | -0.3 | 5.5          | V      |
| Digital input voltage (V1)                                 | V <sub>CTRL</sub>    | -0.3 | 3.6          | V      |
| Maximum input power  | P <sub>MAX,ABS</sub> |      | 41           | dBm    |
| Storage temperature range                                  | T <sub>ST</sub>      | -65  | +150         | °C     |
| ESD voltage HBM <sup>1</sup><br>All pins<br>RF pins to GND | V <sub>ESD,HBM</sub> |      | 1000<br>2500 | V<br>V |
| ESD voltage CDM <sup>2</sup> , all pins                    | V <sub>ESD,MM</sub>  |      | 1000         | V      |

Notes: 1. Human Body Model (MIL-STD 883 Method 3015)  
2. Charged Device Model (JEDEC JESD22-C101)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Table 5. Control Logic Truth Table

| V1 | RFC–RF1 | RFC–RF2 |
|----|---------|---------|
| 0  | OFF     | ON      |
| 1  | ON      | OFF     |

### **Electrostatic Discharge (ESD) Precautions**

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

### **Latch-Up Avoidance**

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

### **Moisture Sensitivity Level**

The Moisture Sensitivity Level rating for the PE42424 in the 6-lead 1.5 × 1.5 mm DFN package is MSL1.

### **Switching Capability**

The PE42424 has a maximum 125 kHz switching rate with the control pin input capacitance of 2 pF. Switching rate describes the time duration between switching events.

Switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

### **Spurious Performance**

The typical spurious performance of the PE42424 is -126 dBm.

Typical Performance Data @ 25 °C and  $V_{DD} = 3.3V$ , unless otherwise specified

Figure 4. Insertion Loss (RFC–RFX)

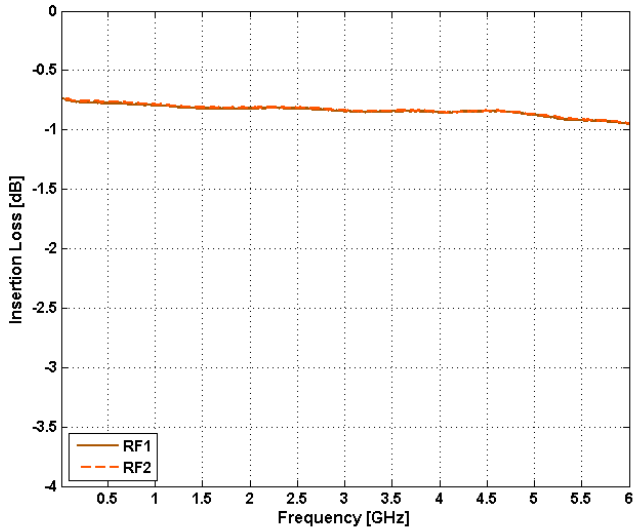


Figure 5. Insertion Loss vs. Temp (RFC–RFX)

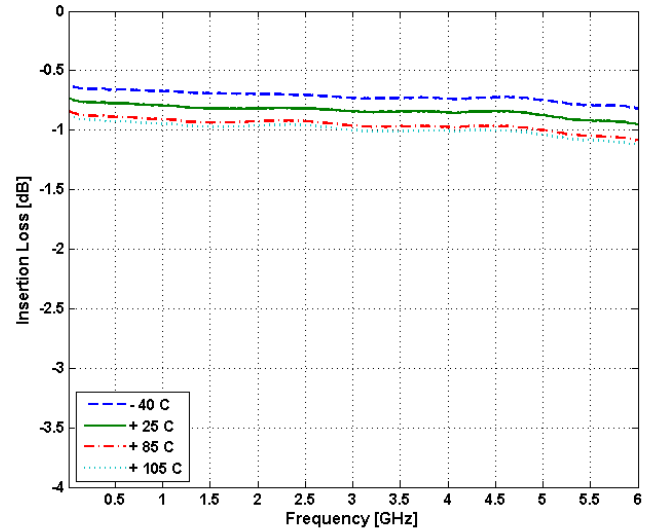
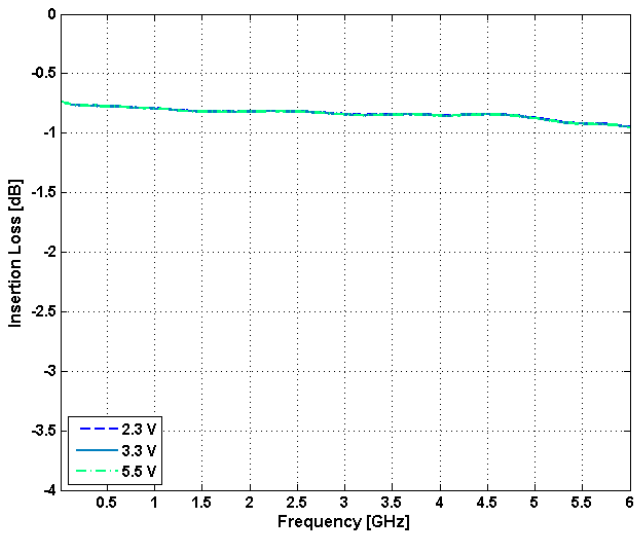


Figure 6. Insertion Loss vs.  $V_{DD}$  (RFC–RFX)



Typical Performance Data @ 25 °C and  $V_{DD} = 3.3V$ , unless otherwise specified

Figure 7. Return Loss vs. Temp (RFC–RFX)

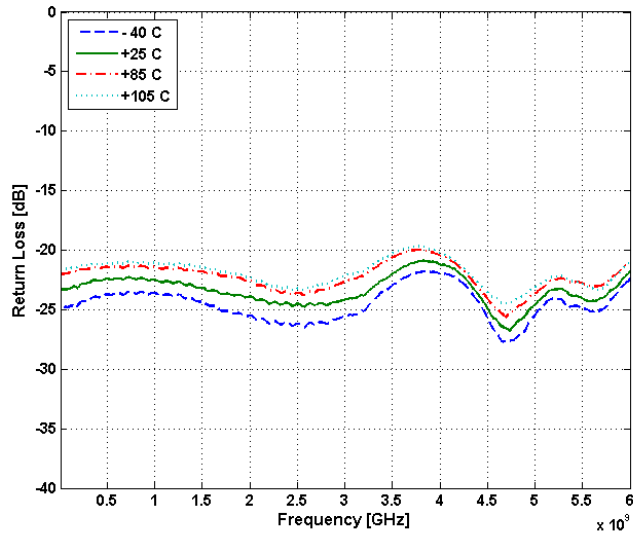


Figure 8. Return Loss vs.  $V_{DD}$  (RFC–RFX)

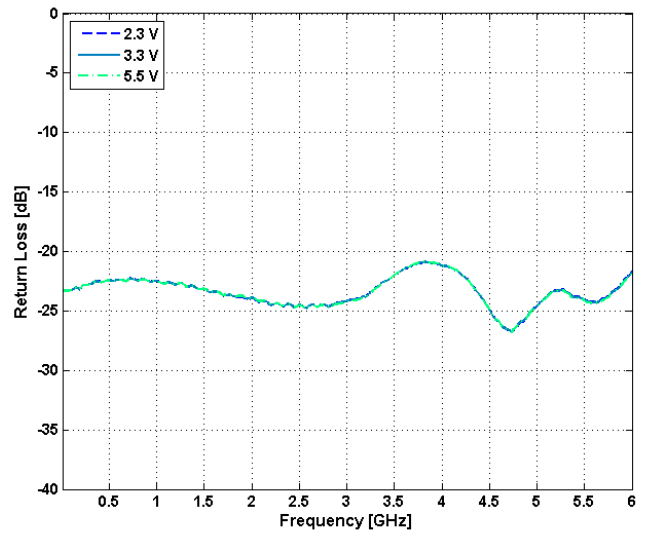


Figure 9. Isolation vs. Temp (RFC–RFX)

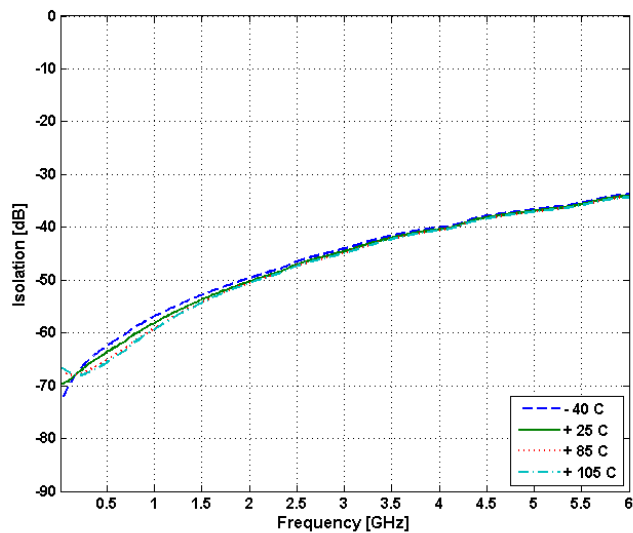
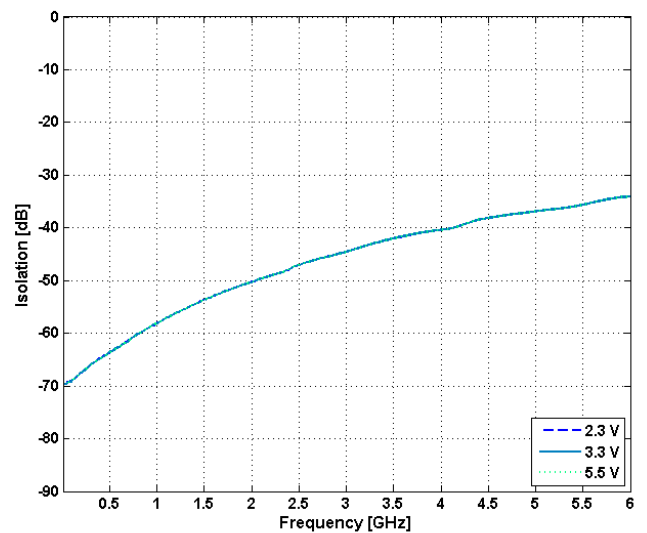


Figure 10. Isolation vs.  $V_{DD}$  (RFC–RFX)



Typical Performance Data @ 25 °C and  $V_{DD} = 3.3V$ , unless otherwise specified

Figure 11. Isolation vs. Temp (RFX–RFX)

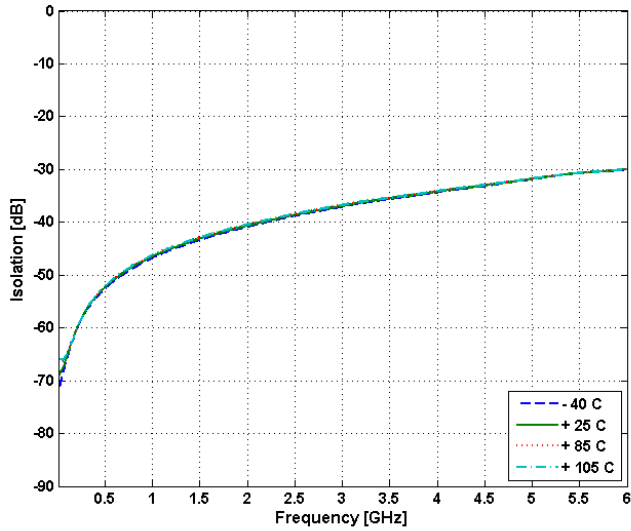
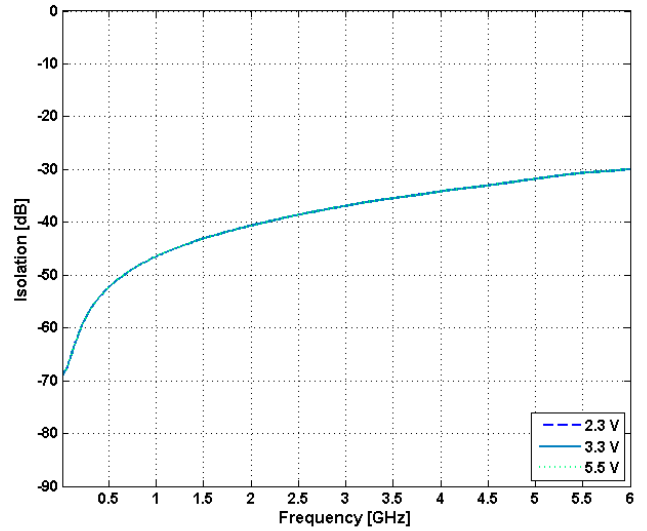


Figure 12. Isolation vs.  $V_{DD}$  (RFX–RFX)



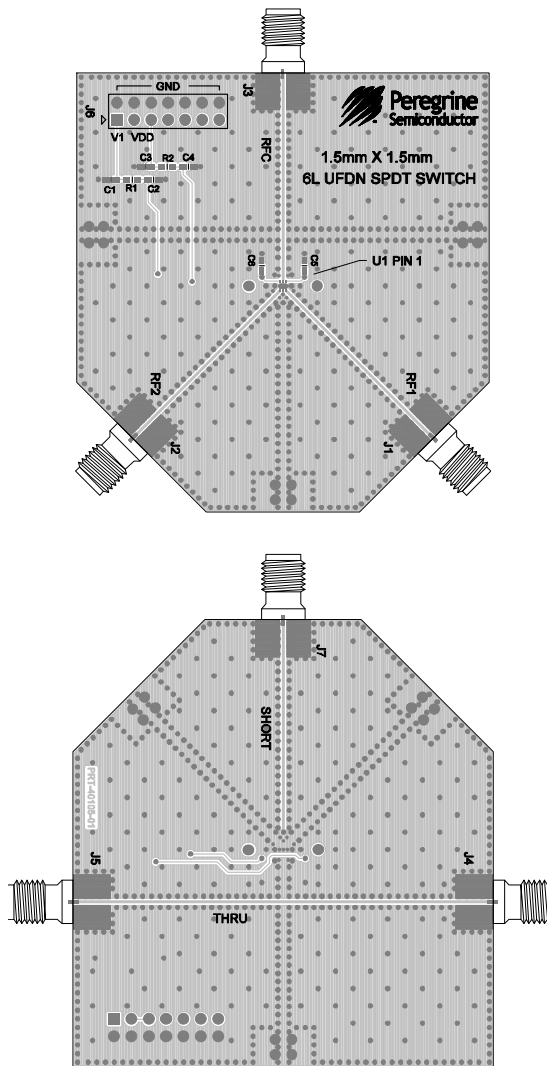
## Evaluation Kit

The SPDT switch evaluation board was designed to ease customer evaluation of Peregrine's PE42424 RF switch. The RF common port is connected to the device through a 50Ω transmission line via SMA connector J3. RF1 and RF2 ports are connected to the device through 50Ω transmission lines via SMA connectors J1 and J2, respectively. A transmission line has been included on the reverse side of the PCB, accessible via SMA connectors J4 and J5. This transmission line provides an equivalent length to de-embed PCB trace losses. DC and digital inputs are provided to the device via J6.

This PCB is constructed of a four metal layer material with total thickness of 62 mils. The top and bottom RF layers are Rogers RO4003 material with an 8 mil RF core. The middle layers provide ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 16 mils and 10 mil trace gap, with 2.1 mils of metal thickness.

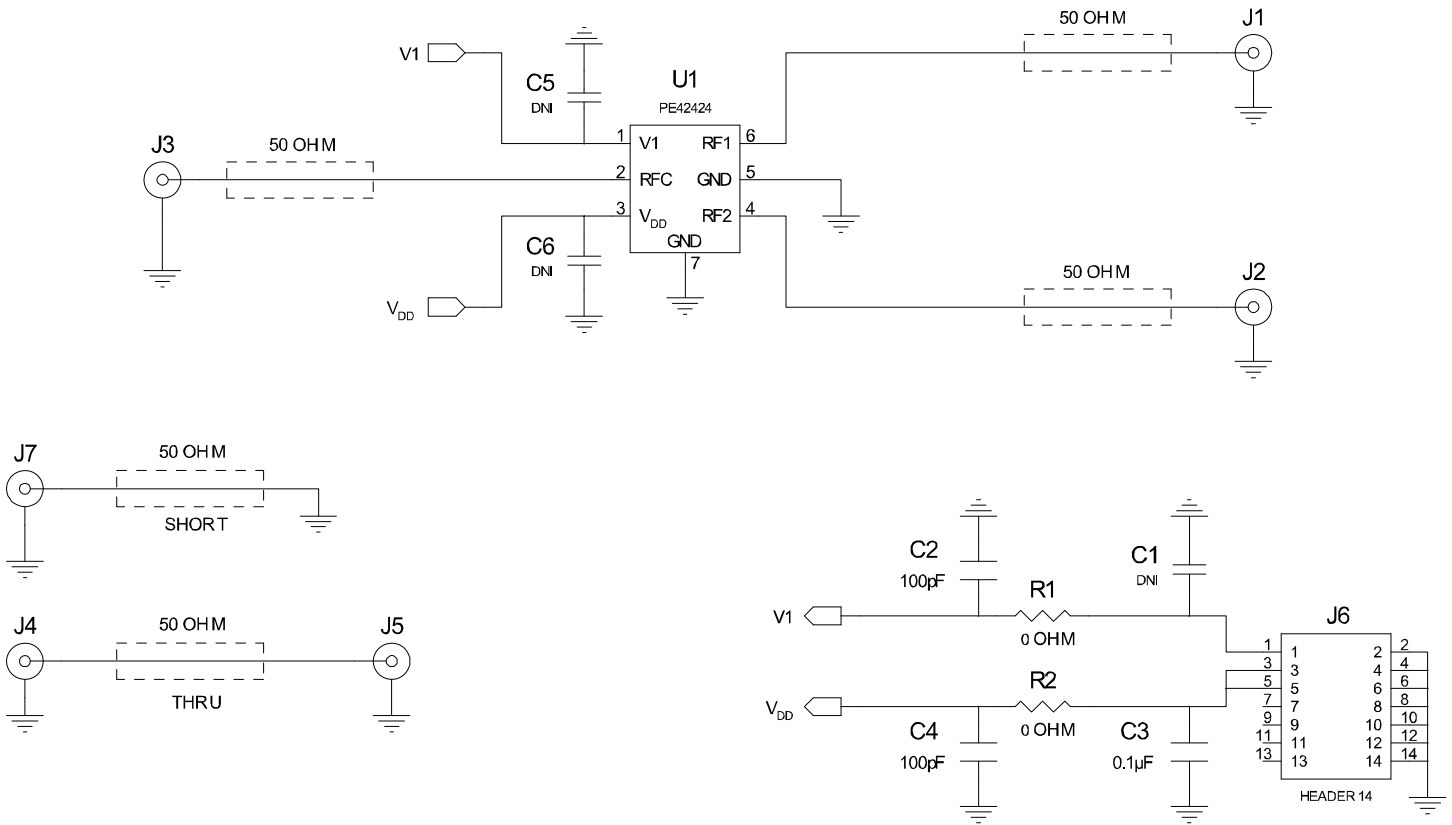
For the true performance of the PE42424 to be realized, the PCB should be designed in such a way that RF transmission lines and sensitive DC I/O traces are heavily isolated from one another.

**Figure 13. Evaluation Board Layout**



PRT-40105

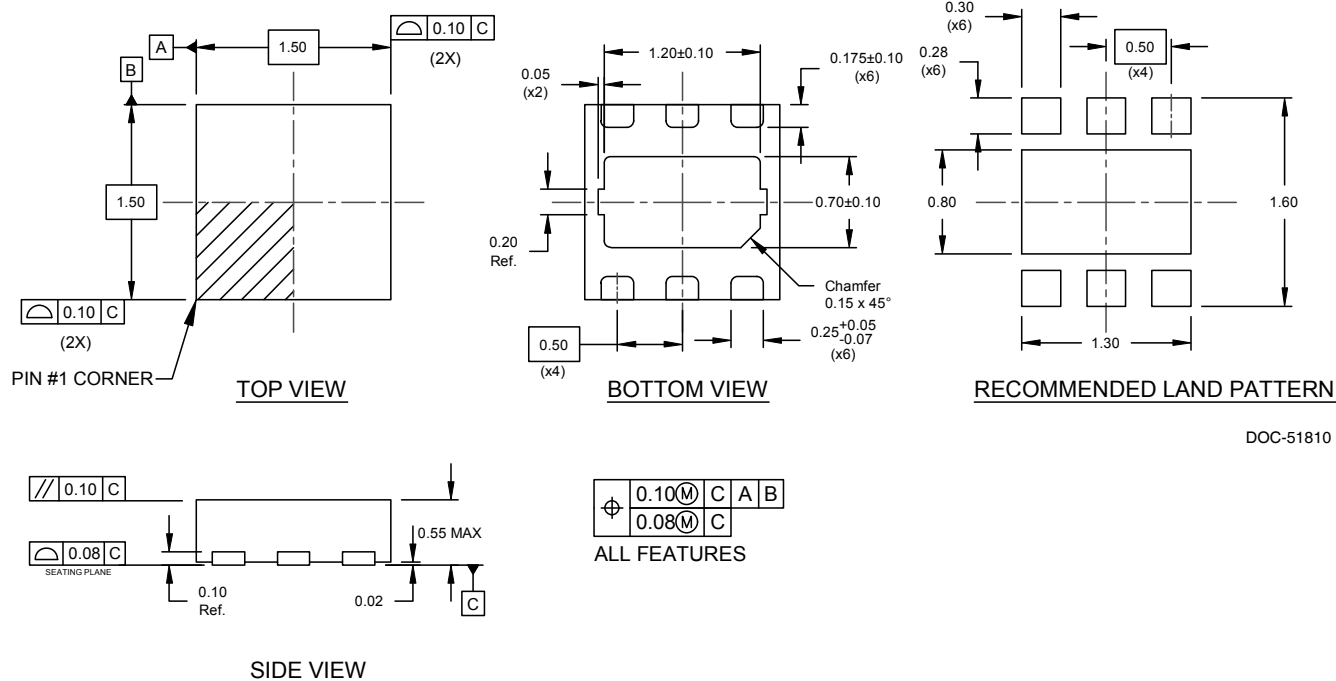
**Figure 14. Evaluation Board Schematic**



CAUTION: Contains parts and assemblies susceptible to damage by electrostatic discharge (ESD).

DOC-44126

**Figure 15. Package Drawing**  
6-lead 1.5 × 1.5 mm DFN



DOC-51810

**Figure 16. Top Marking Specification**

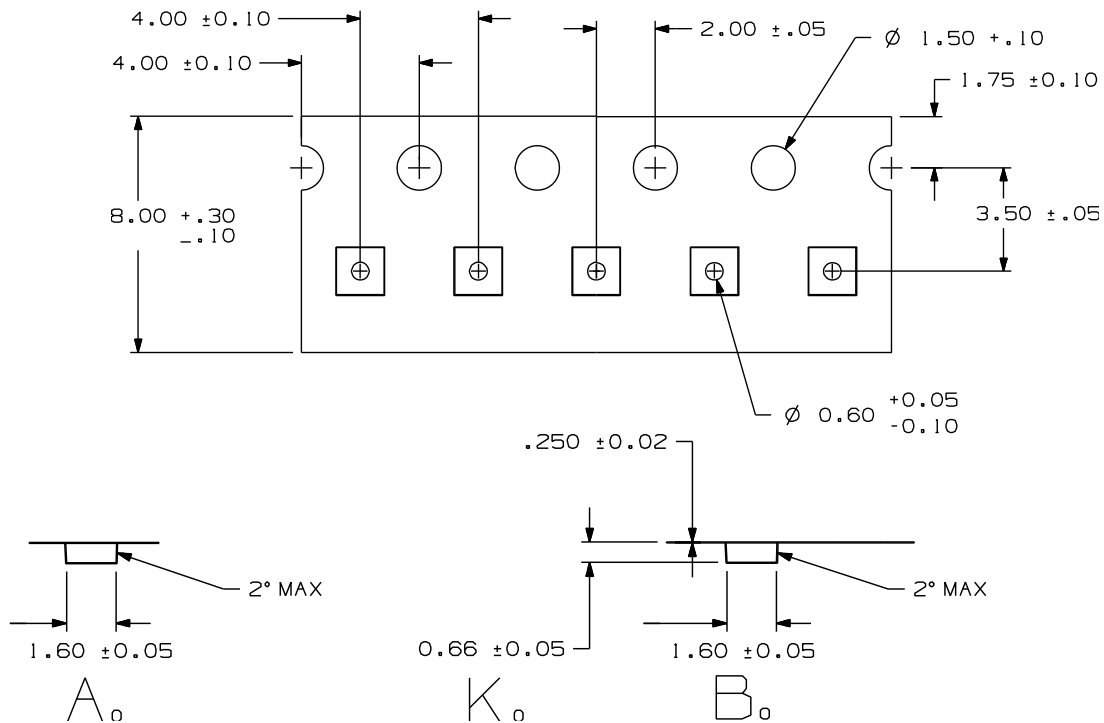


DOC-51207

- = Pin 1 designator
- P = Part number code\*
- ZZ = Last two characters of the assembly lot code
- Y = Last digit of year, starting from 2010
- WW = Work week

Note: \* The part number marking for PE42424 is E.

Figure 17. Tape and Reel Specifications



Drawing not drawn to scale  
Pocket hole diameter  $0.6 \pm 0.05$  mm  
Bumped die are oriented active side down  
Maximum cavity angle  $5^\circ$

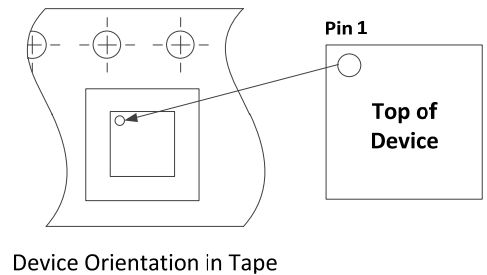


Table 6. Ordering Information

| Ordering Code | Description            | Package                       | Shipping Method |
|---------------|------------------------|-------------------------------|-----------------|
| PE42424A-Z    | PE42424 SPDT RF switch | Green 6-lead 1.5 x 1.5 mm DFN | 3000 units/T&R  |
| EK42424-01    | PE42424 Evaluation kit | Evaluation kit                | 1/Box           |

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