THE DATASHEET OF

SN65LBC184P

TEXAS INSTRUMENTS

SN65LBC184, SN75LBC184

SLLS236I – OCTOBER 1996 – REVISED JUNE 2015

SNx5LBC184 Differential Transceiver With Transient Voltage Suppression

1 Features

- Integrated Transient Voltage Suppression
- ESD Protection for Bus Terminals Exceeds:
  ±30 kV IEC 61000-4-2, Contact Discharge
  ±15 kV IEC 61000-4-2, Air-Gap Discharge
  ±15 kV EIA/JEDEC Human Body Model
- Circuit Damage Protection of 400-W Peak (Typical) Per IEC 61000-4-5
- Controlled Driver Output-Voltage Slew Rates Allow Longer Cable Stub Lengths
- 250-kbps in Electrically Noisy Environments
- Open-Circuit Fail-Safe Receiver Design
- 1/4 Unit Load Allows for 128 Devices Connected on Bus
- Thermal Shutdown Protection
- Power-Up and Power-Down Glitch Protection
- Each Transceiver Meets or Exceeds the Requirements of TIA/EIA-485 (RS-485) and ISO/IEC 8482:1993(E) Standards
- Low Disabled Supply Current 300 µA Maximum
- Pin Compatible With SN75176

2 Applications

- Industrial Networks
- Utility Meters
- Motor Control

3 Description

The SN75LBC184 and SN65LBC184 devices are differential data line transceivers in the trade-standard footprint of the SN75176 with built-in protection against high-energy noise transients. This feature provides a substantial increase in reliability for better immunity to noise transients coupled to the data cable over most existing devices. Use of these circuits provides a reliable low-cost direct-coupled (with no isolation transformer) data line interface without requiring any external components.

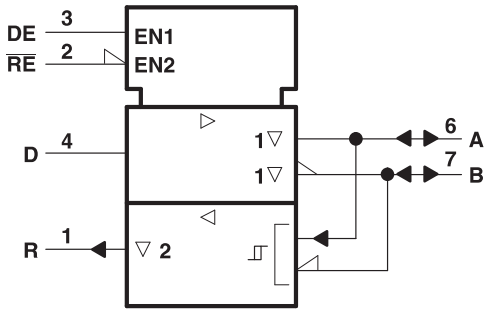
The SN75LBC184 and SN65LBC184 can withstand overvoltage transients of 400-W peak (typical). The conventional combination wave called out in IEC 61000-4-5 simulates the overvoltage transient and models a unidirectional surge caused by overvoltages from switching and secondary lightning transients.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65LBC184, SN75LBC184	SOIC (8)	4.90 mm × 3.91 mm
	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Logic Symbol



NOTE: This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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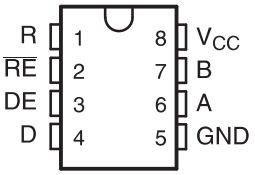
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (February 2009) to Revision I	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

D Package, P Package
8-Pin SOIC, 8-Pin PDIP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Active-HIGH driver enable
GND	5	Reference potential	Local device ground
R	1	Digital output	Receiver data output
$\overline{RE}$	2	Digital input	Active-LOW receiver enable
V_{CC}	8	Supply	4.75-V to 5.25-V supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	–0.5	7	V
	Continuous voltage range at any bus terminal	–15	15	V
	Data input/output voltage	–0.3	7	V
I_O	Receiver output current	–20	20	mA
	Continuous total power dissipation(3)	Internally Limited		
T_{stg}	Storage temperature		160	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
(3) The driver shuts down at a junction temperature of approximately 160°C. To operate below this temperature, see the *Dissipation Ratings*.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	A, B, GND	±15000	V
			All pins	±3000	
		Contact discharge (IEC61000-4-2)	A, B, GND(2)	±30000	
		Air discharge (IEC61000-4-2)	A, B, GND(3)	±15000	
		All pins (Class 3A)		±8000	
		All pins (Class 3B)		±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) GND and bus pin ESD protection is beyond readily available test equipment capabilities for IEC 61000-4-2, EIA/JEDEC test method A114-A and MIL-STD-883C method 3015. Ratings listed are limits of test equipment; device performance exceeds these limits.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN(1)	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–7		12	V
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
$\|V_{ID}\|$	Differential input voltage				12	V
I_{OH}	High-level output current	Driver	–60			mA
		Receiver	–8			
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			4	
T_A	Operating free-air temperature	SN75LBC184	0		70	°C
		SN65LBC184	–40		85	

(1) The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet.

6.4 Thermal Information

THERMAL METRIC(1)		SNx5LBC184		UNIT
		P [PDIP]	D [SOIC]	
		8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.7	172.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.8	42.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.6	41.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12	4.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.5	40.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		ALTERNATE SYMBOLS	TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current	NA	DE = $\overline{RE}$ = 5 V	No Load		12	25	mA
			DE = 0 V, $\overline{RE}$ = 5 V	No Load		175	300	µA
I_{IH}	High-level input current (D, DE, $\overline{RE}$)	NA	V_I = 2.4 V				50	µA
I_{IL}	Low-level input current (D, DE, $\overline{RE}$)	NA	V_I = 0.4 V		–50			µA
I_{OS}	Short-circuit output current OS(2)	NA	V_O = –7 V		–250	–120		mA
			V_O = V_{CC}				250	
			V_O = 12 V				250	
I_{OZ}	High-impedance output current	NA	See Receiver I_I					mA
V_O	Output voltage	V_{oa}, V_{ob}	I_O = 0		0		V_{CC}	V
$V_{OC(PP)}$	Peak-to-peak change in common-mode output voltage during state transitions	NA	See Figure 9 and Figure 10			0.8		V
V_{OC}	Common-mode output voltage	$\lvert V_{os}\rvert$	See Figure 8		1		3	V
$\lvert\Delta V_{OC(SS)}\rvert$	Magnitude of change, common-mode steady-state output voltage	$\lvert V_{os} - V_{os}\rvert$	See Figure 10				0.1	V
$\lvert V_{OD}\rvert$	Magnitude of differential output voltage $\lvert V_A - V_B\rvert$	V_o	I_O = 0		1.5		6	V
			R_L = 54 Ω, See Figure 8		1.5			V
$\Delta\lvert V_{OD}\rvert$	Change in differential voltage magnitude between logic states	$\lVert V_t\rvert - \lvert V_t\rVert$	R_L = 54 Ω				0.1	V

(1) All typical values are measured with T_A = 25°C and V_{CC} = 5 V.
(2) This parameter is measured with only one output being driven at a time.

6.6 Electrical Characteristics: Receiver

over recommended operation conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current (total package)	DE = $\overline{RE}$ = 0 V, No Load				3.9	mA
		$\overline{RE}$ = 5 V, DE = 0 V, No Load				300	µA
I_I	Input current	Other input = 0 V	V_I = 12 V			250	µA
			V_I = 12 V, V_{CC} = 0			250	
			V_I = –7 V	–200			
			V_I = –7 V, V_{CC} = 0	–200			
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±100	µA
V_{hys}	Input hysteresis voltage				70		mV
V_{IT+}	Positive-going input threshold voltage					200	V
$V_{IT–}$	Negative-going input threshold voltage			–200			mV
V_{OH}	High-level output voltage	I_{OH} = –8 mA, See Figure 11		2.8			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 11				0.4	V

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

6.7 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(DH)}$	Differential output delay time, low-to-high-level output	R_L = 54 Ω, C_L = 50 pF	See Figure 9			1.3	µs
$t_{d(DL)}$	Differential output delay time, high-to-low-level output					1.3	µs
t_{PLH}	Propagation delay time, low-to-high-level output				0.5	1.3	µs
t_{PHL}	Propagation delay time, high-to-low-level output				0.5	1.3	µs
$t_{sk(p)}$	Pulse skew (| $t_{d(DH)} - t_{d(DL)}$ |)				75	150	ns
t_r	Rise time, single-ended			0.25		1.2	µs
t_f	Fall time, single-ended			0.25		1.2	µs
t_{PZH}	Output enable time to high level	R_L = 110 Ω	See Figure 6			3.5	µs
t_{PZL}	Output enable time to low level	R_L = 110 Ω	See Figure 7			3.5	µs
t_{PHZ}	Output disable time from high level	R_L = 110 Ω	See Figure 6			2	µs
t_{PLZ}	Output disable time from low level	R_L = 110 Ω	See Figure 7			2	µs

6.8 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, See Figure 11			150	ns
t_{PHL}	Propagation delay time, high-to-low-level output				150	ns
$t_{sk(p)}$	Pulse skew (|t_{PHL} – t_{PLH}|)				50	ns
t_r	Rise time, single-ended	See Figure 11		20		ns
t_f	Fall time, single-ended			20		ns
t_{PZH}	Output enable time to high level	See Figure 12			100	ns
t_{PZL}	Output enable time to low level				100	ns
t_{PHZ}	Output disable time from high level				100	ns
t_{PLZ}	Output disable time from low level				100	ns

6.9 Dissipation Ratings

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1150 mW	9.2 mW/°C	736 mW	598 mW

6.10 Typical Characteristics

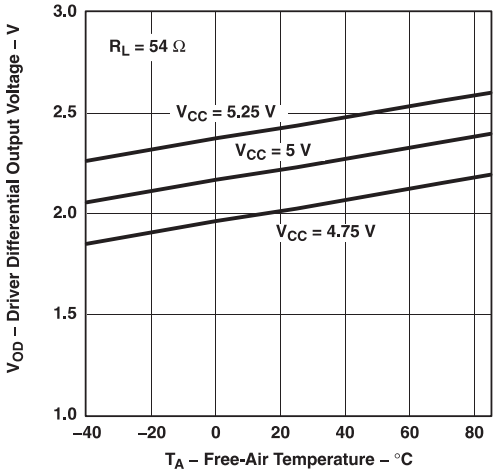


Figure 1. Driver Differential Output Voltage vs Free-Air Temperature

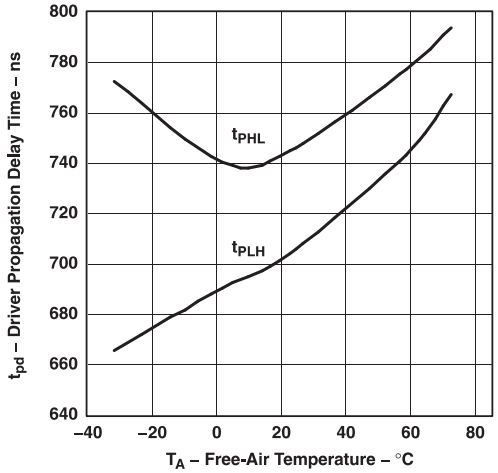


Figure 2. Driver Propagation Delay Time vs Free-Air Temperature

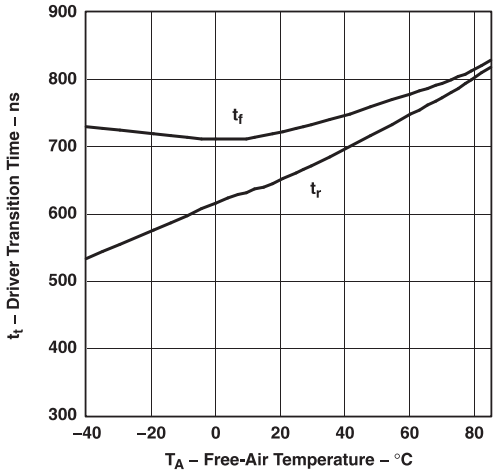


Figure 3. Driver Transition Time vs Free-Air Temperature

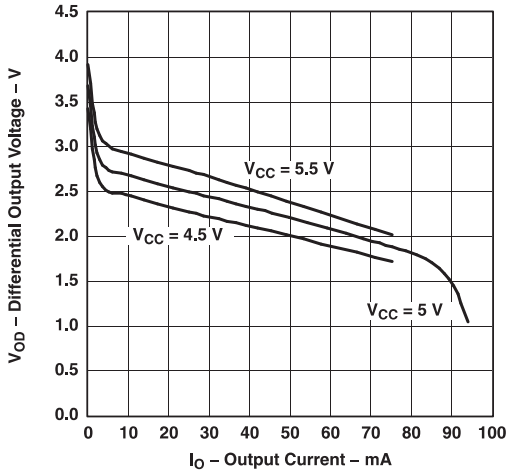


Figure 4. Differential Output Voltage vs Output Current

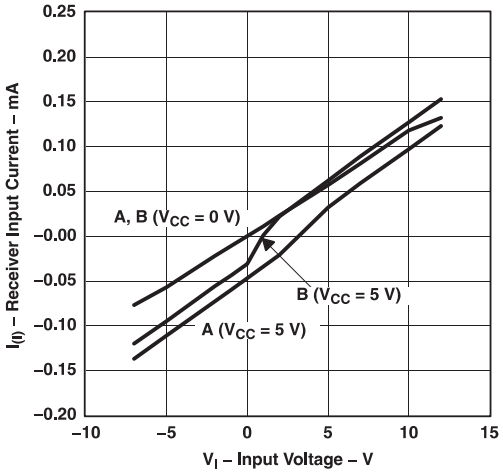
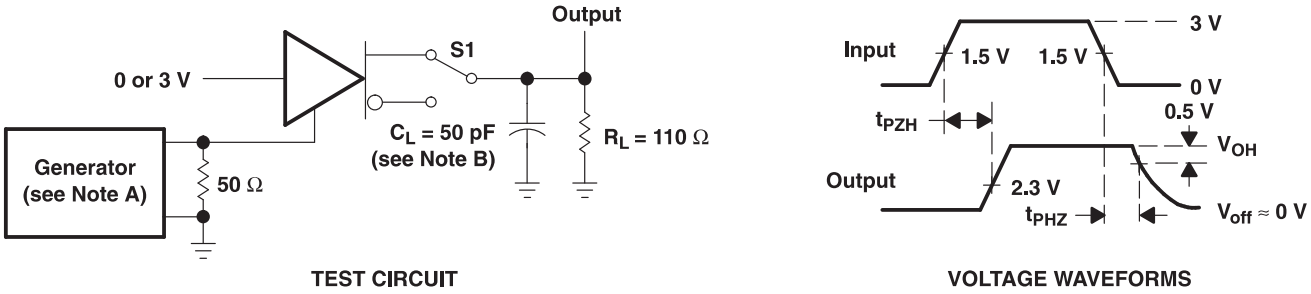


Figure 5. Receiver Input Current vs Input Voltage

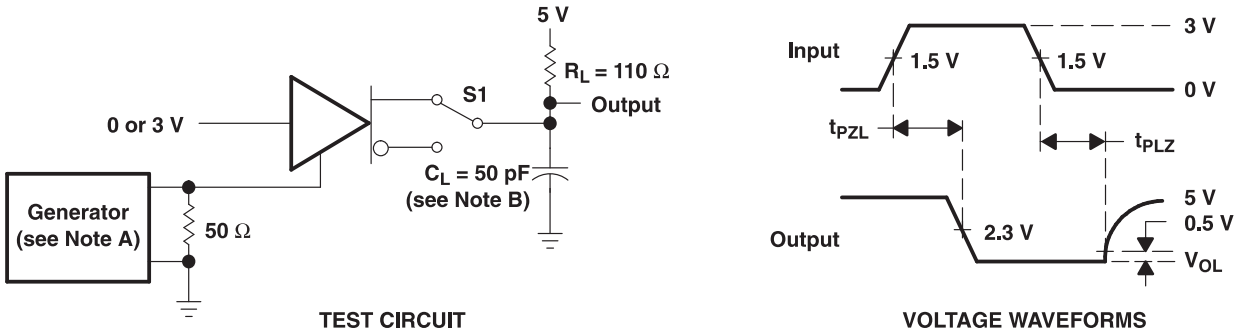
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

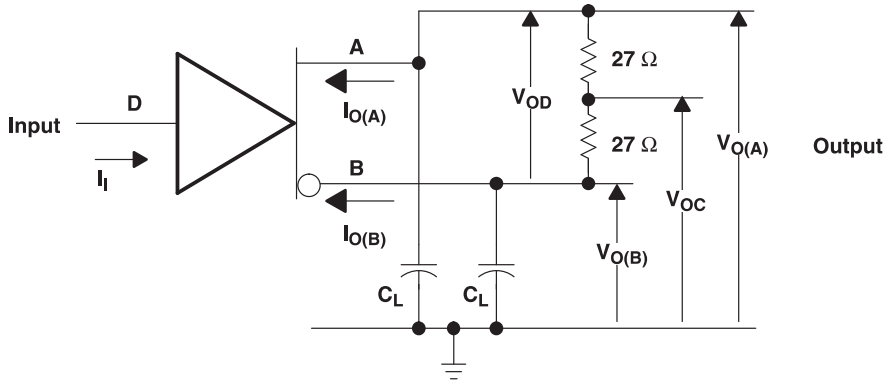
Figure 6. Driver t_{PZH} and t_{PHZ} Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

Figure 7. Driver t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms



A. Resistance values are in ohms and are 1% tolerance.

B. C_L includes probe and jig capacitance.

Figure 8. Driver Test Circuit, Voltage, and Current Definitions

Parameter Measurement Information (continued)

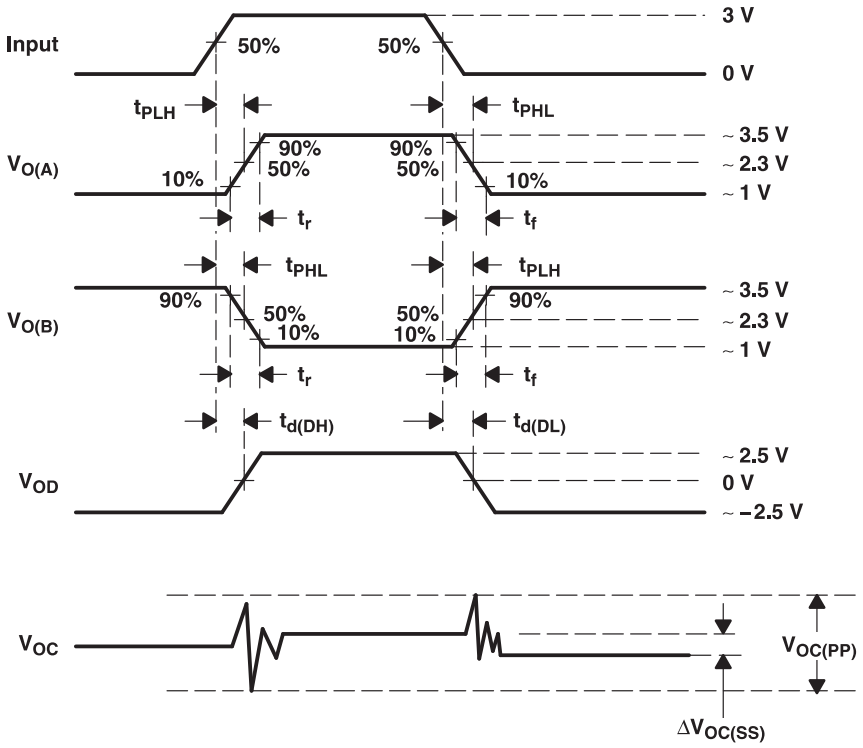
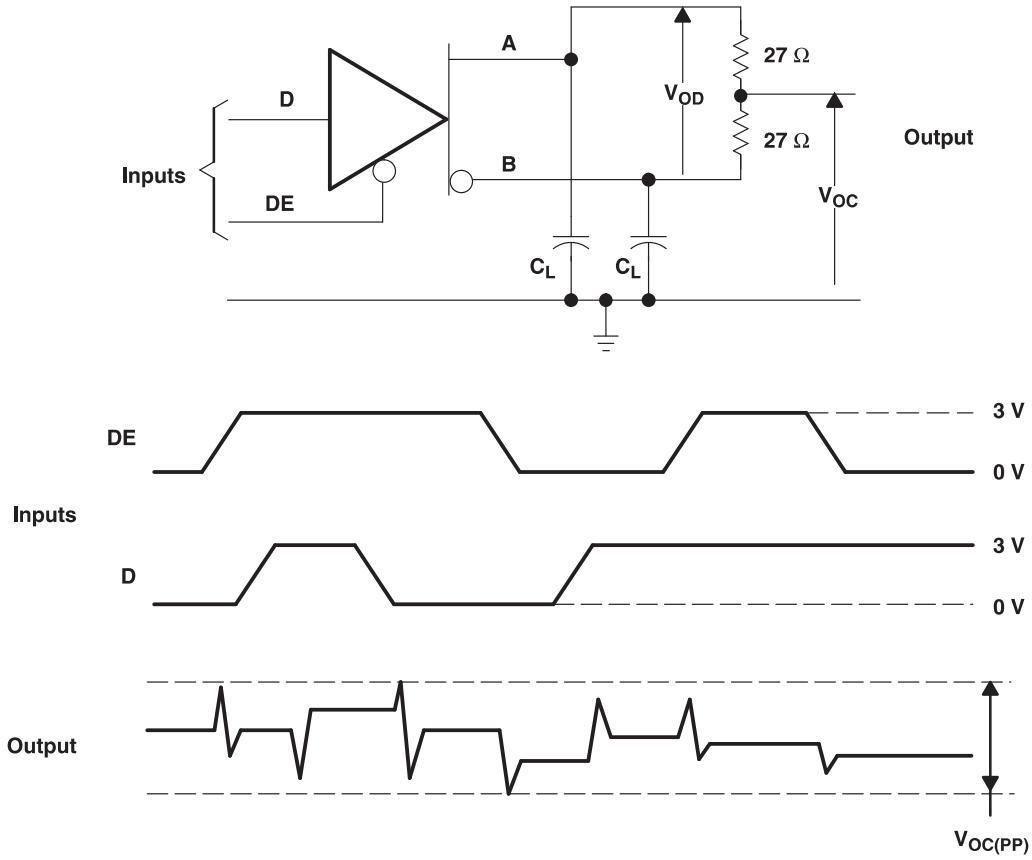


Figure 9. Driver Timing, Voltage, and Current Waveforms

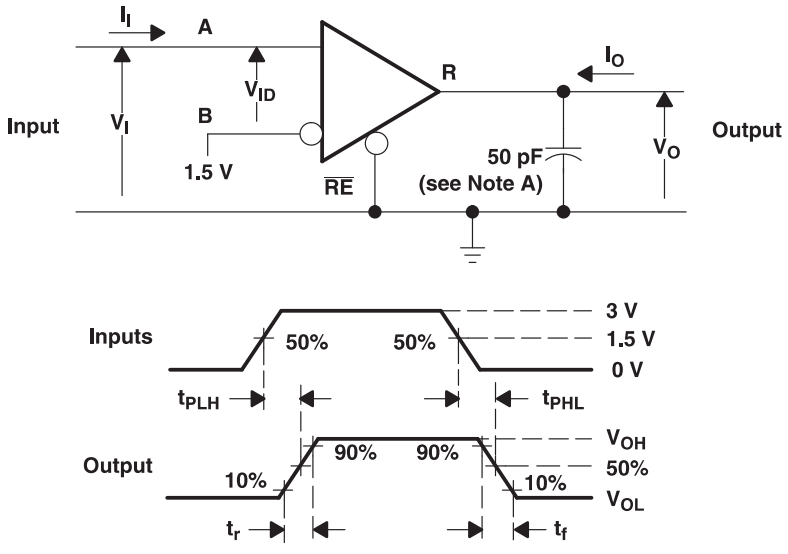
Parameter Measurement Information (continued)



A. Resistance values are in ohms and are 1% tolerance.

B. C_L includes probe and jig capacitance (±10%).

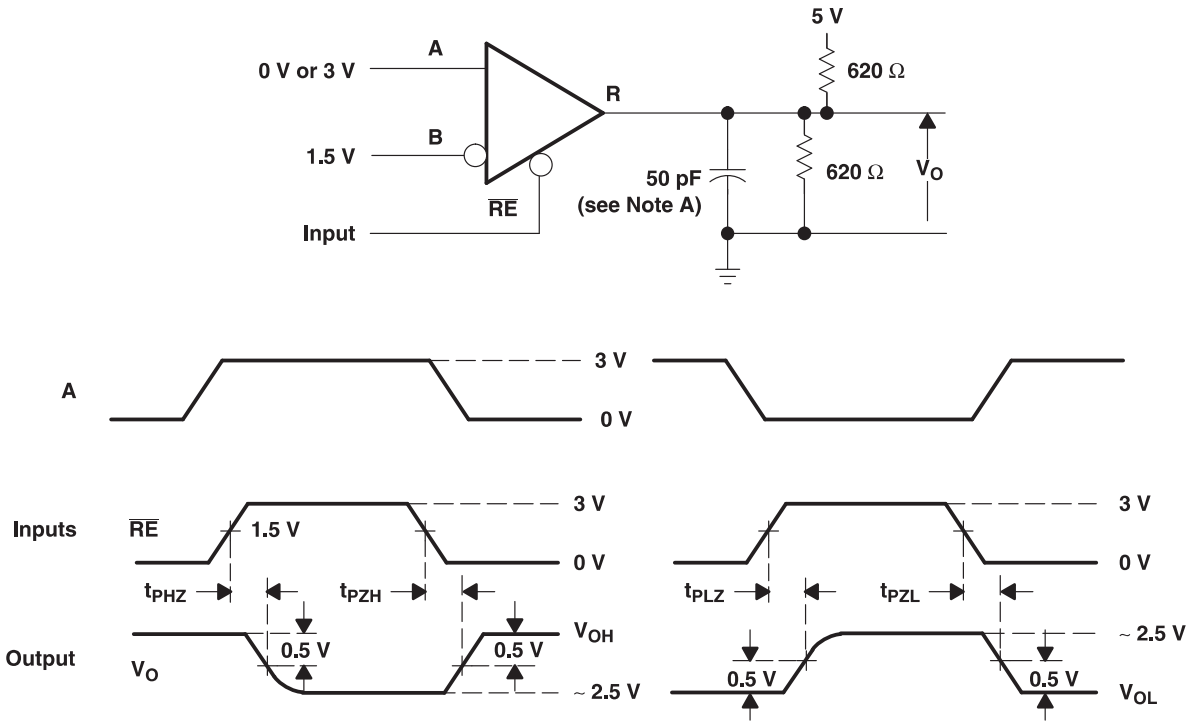
Figure 10. Driver $V_{OC(PP)}$ Test Circuit and Waveforms



A. This value includes probe and jig capacitance (±10%).

Figure 11. Receiver t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



A. This value includes probe and jig capacitance (±10%).

Figure 12. Receiver t_{PZL}, t_{PLZ}, t_{PZH}, and t_{PHZ} Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SNx5LBC184 device is a 5-V, half-duplex, RS-485 transceiver with integrated transient voltage suppressors that prevent circuit damage in the presence of high-energy transients of up to 400-W peak power. This transceiver has an active-HIGH driver enable and active-LOW receiver enable. The differential driver is suitable for data transmission up to 250 kbps.

8.2 Functional Block Diagram

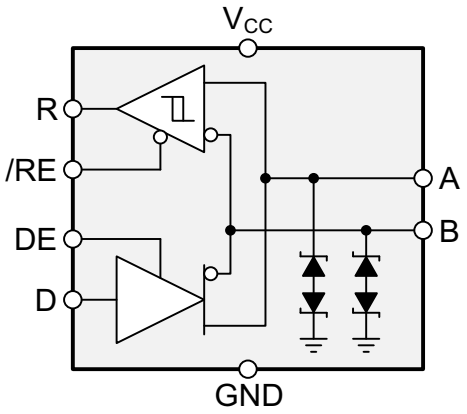


Figure 13. Functional Logic Diagram

8.3 Feature Description

Integrated transient voltage suppressors protect the transceiver against Electrostatic Discharges (ESD) according to IEC 61000-4-2 of up to ±30 kV and surge transients according to IEC 61000-4-5 of up to 400-W peak.

The differential driver incorporates slew-rate controlled outputs sufficient to transmit data up to 250 kbps. Slew-rate control allows for longer unterminated cable runs and longer stub lengths from the main cable trunk than with faster voltage transitions. A unique receiver design provides a high level failsafe output when the inputs are left floating.

The SN65LBC184 is characterized from –40°C to 85°C and the SN75LBC184 is characterized from 0°C to 70°C.

8.4 Device Functional Modes

When the driver enable pin (DE) is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition, the logic state at D is irrelevant.

Table 1. Driver Functions(1)

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output (R) turns high. When V_{ID} is negative and lower than the negative input threshold, V_{IT-}, the receiver output turns low. If V_{ID} is between V_{IT+} and V_{IT-}, the output is indeterminate.

When $\overline{RE}$ is logic high, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. When the transceiver is disconnected from the bus, the receiver provides a failsafe high output.

Table 2. Receiver Functions(1)

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{ID} > V_{IT+}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
OPEN	L	H	Receiver failsafe High

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

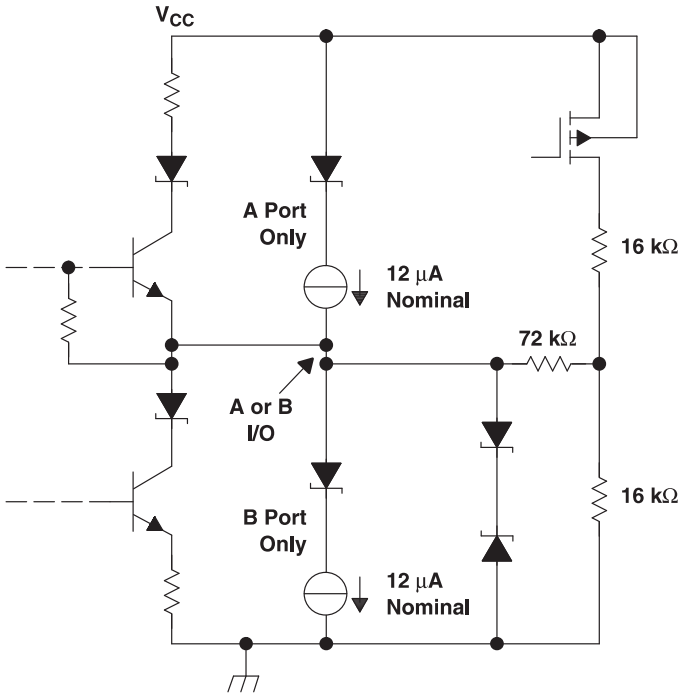


Figure 14. Schematic of Inputs and Outputs

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN65LBC184 and SN75LBC184 devices are half-duplex, RS-485 transceivers commonly used for asynchronous data transmissions. The driver and receiver enable pins allow for the configuration of different operating modes.

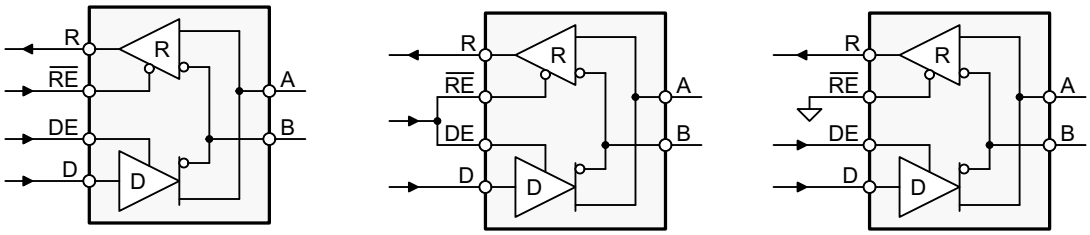


Figure 15. Half-Duplex Transceiver Configurations

a. Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.
b. Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high, and as a receiver when the direction-control line is low.
c. Only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node not only receives the data from the bus, but also the data it sends and can verify that the correct data have been transmitted.

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connected in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over a longer cable length.

Typical Application (continued)

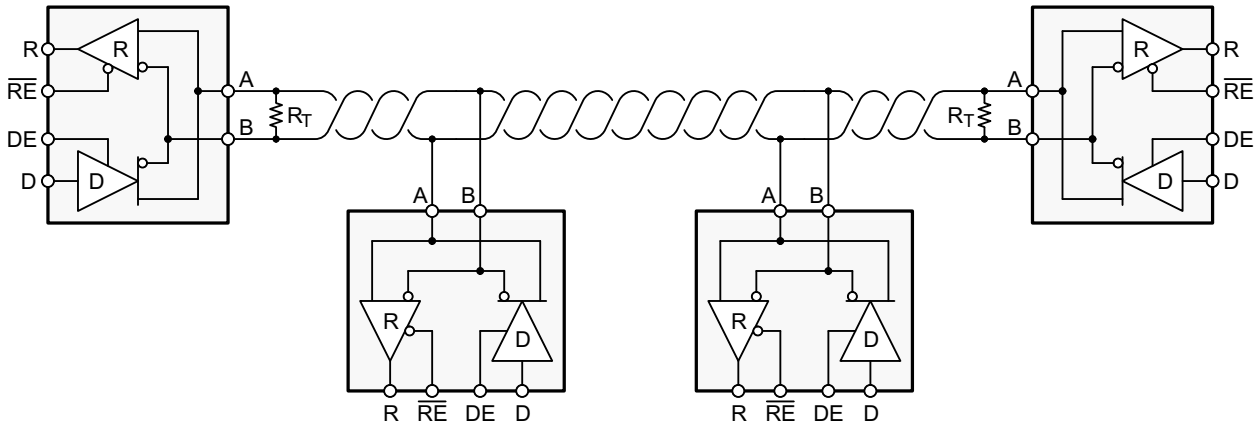


Figure 16. Typical RS-485 Network With Half-Duplex Transceivers

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, meaning the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable may be without introducing data errors. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

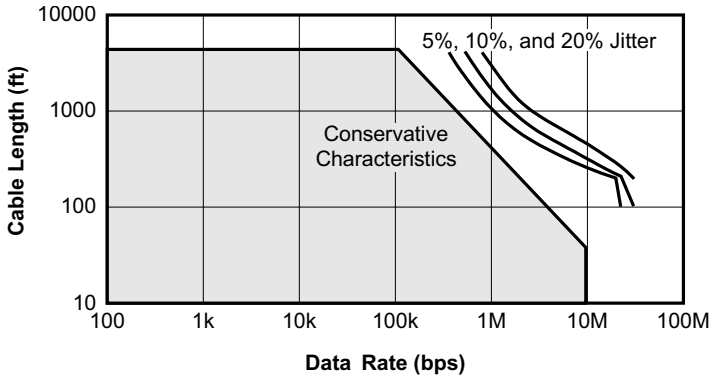


Figure 17. Cable Length vs Data Rate Characteristic

Typical Application (continued)

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a nonterminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- v is the signal velocity of the cable or trace as a factor of c
- c is the speed of light (3×10^8 m/s)

Per Equation 1, cable-stub lengths when using the SN65LBC184 driver must be not greater than 5.85 meters (19 feet) for a signal velocity of 78% and minimum driver output rise or fall time of 250 ns.

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the SN65LBC184 is a 1/4 UL transceiver, it is possible to connect up to 128 receivers to the bus.

9.2.2 Detailed Design Procedure

9.2.2.1 SN65LBC184 Test Description

The SN65LBC184 is tested against the IEC 61000-4-5 recommended transient identified as the combination wave. The combination wave provides a 1.2-/50-µs open-circuit voltage waveform and a 8-/20-µs short-circuit current waveform shown in Figure 18. The testing is performed with a combination/hybrid pulse generator with an effective output impedance of 2 Ω. The setup for the overvoltage stress is shown in Figure 19 with all testing performed with power applied to the SN65LBC184 circuit.

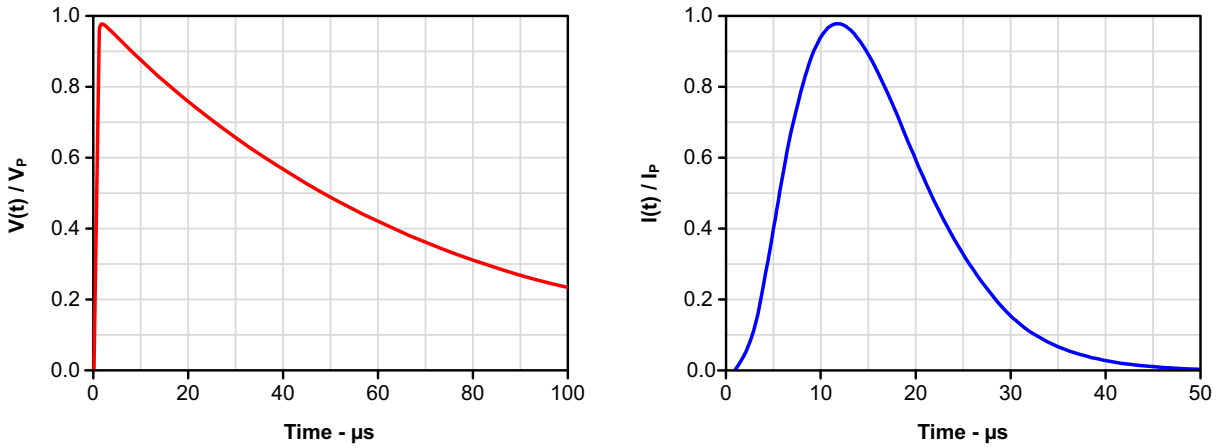


Figure 18. Open-Circuit Voltage and Short-Circuit Current Waveforms

The SN65LBC184 is tested and evaluated for both maximum (single pulse) as well as life test (multiple pulse) capabilities. The SN65LBC184 is evaluated against transients of both positive and negative polarity and all testing is performed with the worst-case transient polarity. Transient pulses are applied to the bus pins (A and B) across ground as shown in Figure 19.

Typical Application (continued)

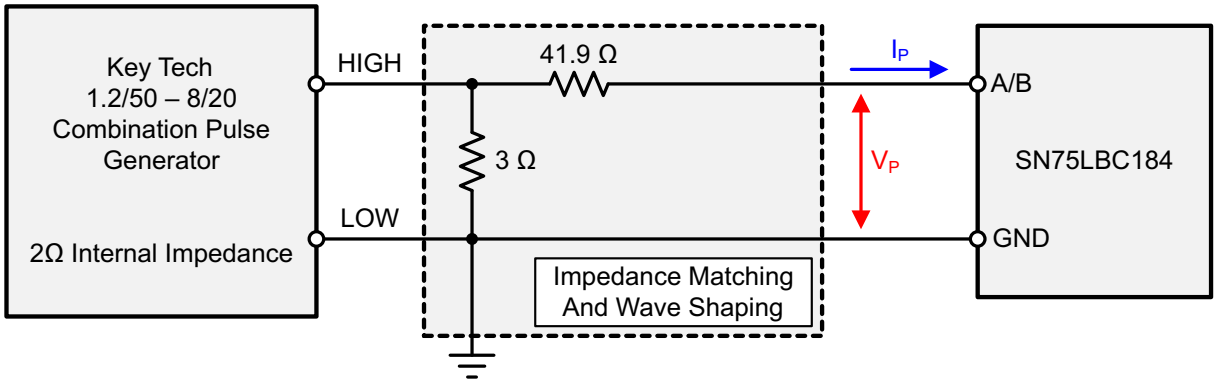


Figure 19. Overvoltage Stress Test Circuit

9.2.3 Application Curve

An example waveform as seen by the SN65LBC184 is shown in Figure 20. The bottom trace is current, the middle trace shows the clamping voltage of the device and the top trace is power as calculated from the voltage and current waveforms. This example shows a peak clamping voltage of 33.6 V and peak current of 16 A, thus yielding an absorbed peak power of 538 W.

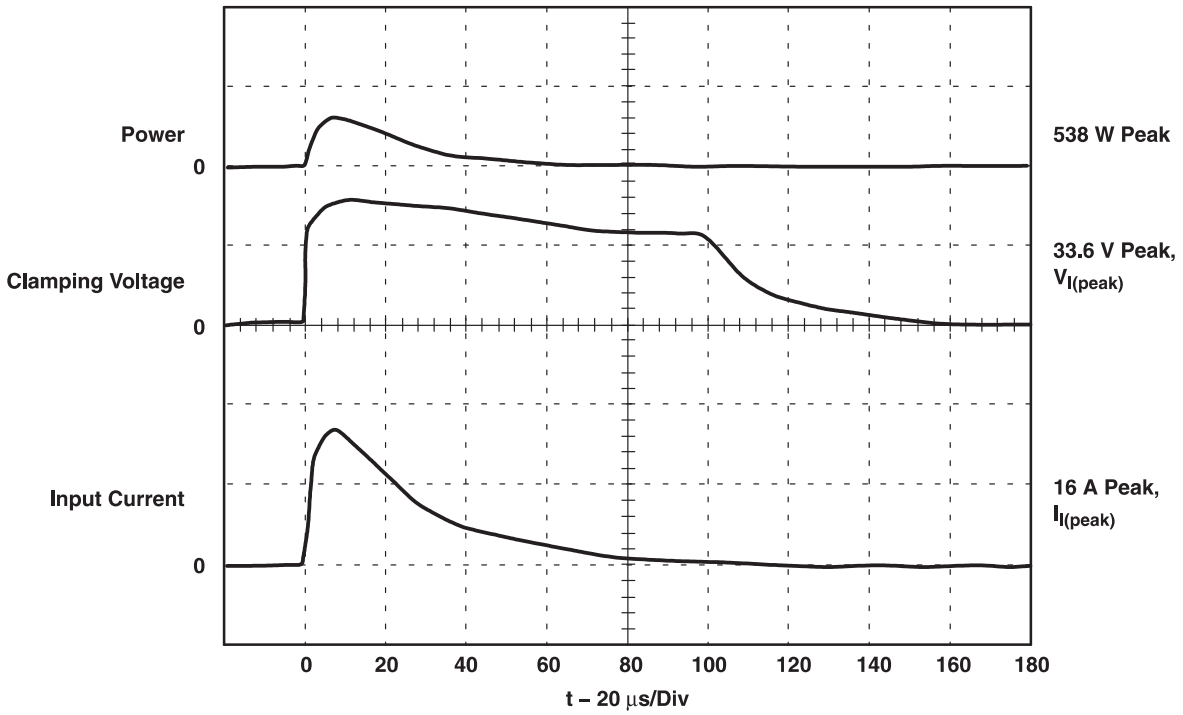


Figure 20. Typical Surge Waveform Measured at Pins 5 and 7

10 Power Supply Recommendations

To assure reliable operation at all data rates and supply voltages, each supply should be buffered with a 100-nF ceramic capacitor located as close to the supply pins as possible. The TPS76350 is a linear voltage regulator suitable for the 5-V supply.

11 Layout

11.1 Layout Guidelines

Because ESD transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design.

- Use V_{CC} and ground planes to provide low inductance. High frequency currents follow the path of least inductance and not the path of least impedance.
- Apply 100-nF to 220-nF bypass capacitors as close as possible to the V_{CC} pins of transceiver, UART, or controller ICs on the board.
- Use at least two vias for V_{CC} and ground connections of bypass capacitors to minimize effective via-inductance.
- Use 1-kΩ to 10-kΩ pullup or pulldown resistors for enable lines to limit noise currents in these lines during transient events.

11.2 Layout Example

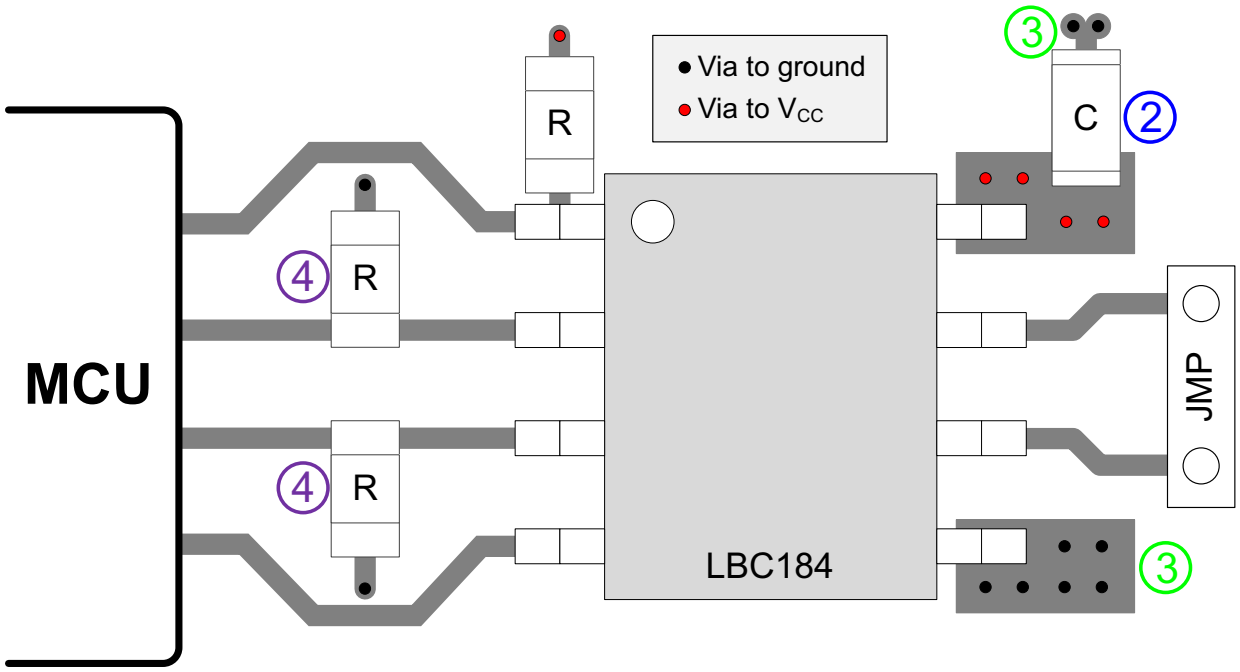


Figure 21. Layout Schematic

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65LBC184	Click here	Click here	Click here	Click here	Click here
SN75LBC184	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC184D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB184	
SN65LBC184DG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB184	
SN65LBC184DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB184	Samples
SN65LBC184DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB184	Samples
SN65LBC184P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65LBC184	Samples
SN75LBC184D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB184	
SN75LBC184DG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB184	
SN75LBC184DR	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB184	
SN75LBC184DRG4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB184	
SN75LBC184P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75LBC184	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

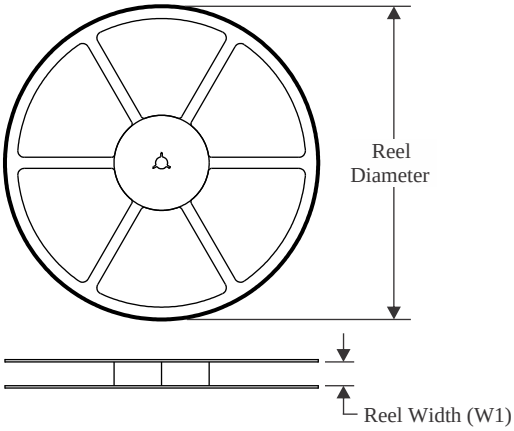
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

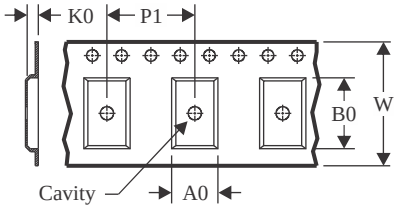
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

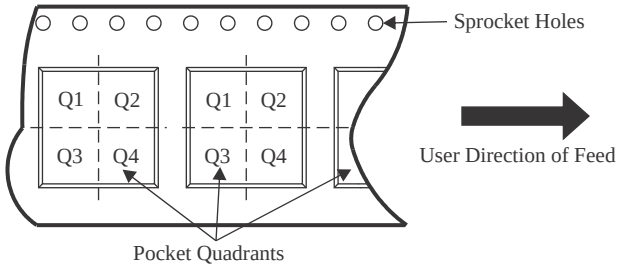


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

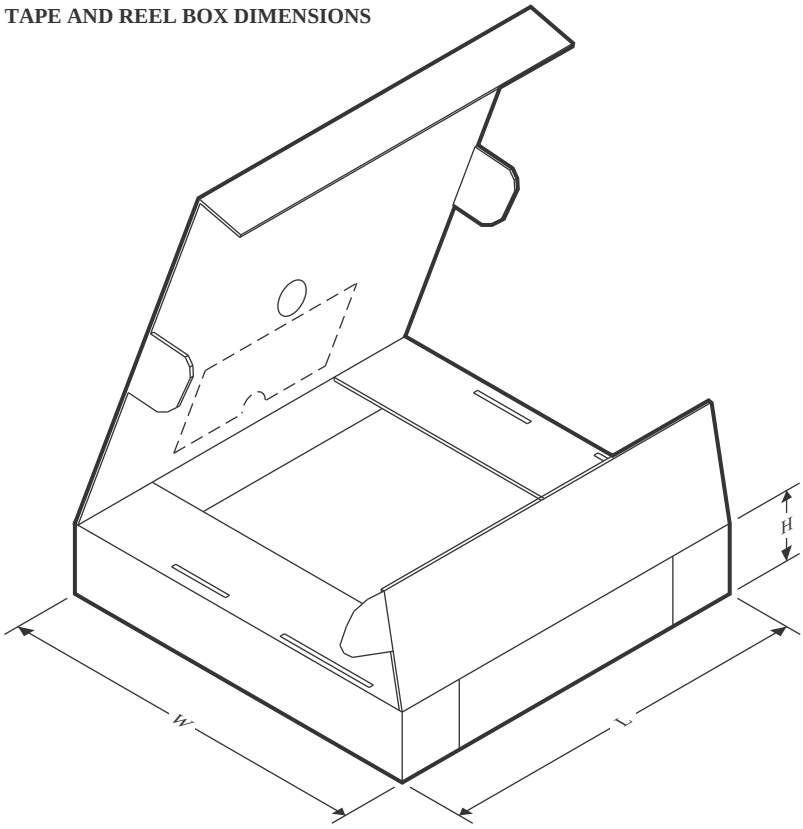
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC184DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC184DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

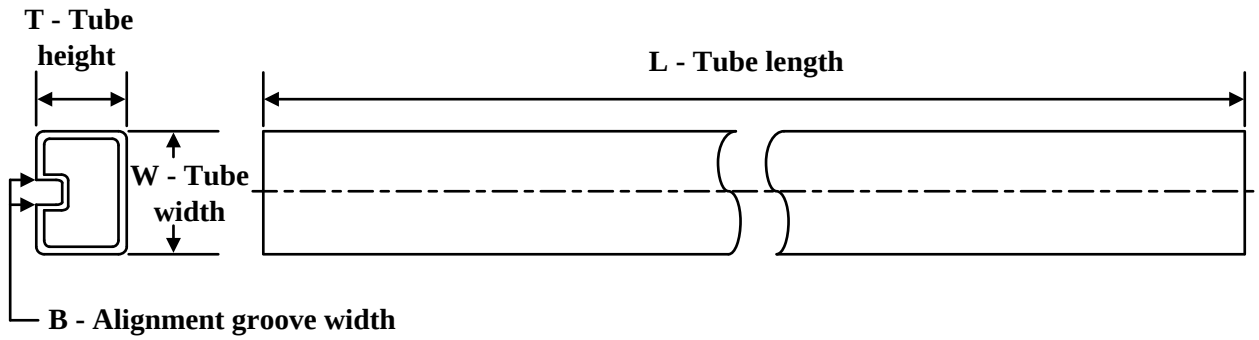
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC184DR	SOIC	D	8	2500	340.5	338.1	20.6
SN75LBC184DR	SOIC	D	8	2500	340.5	338.1	20.6

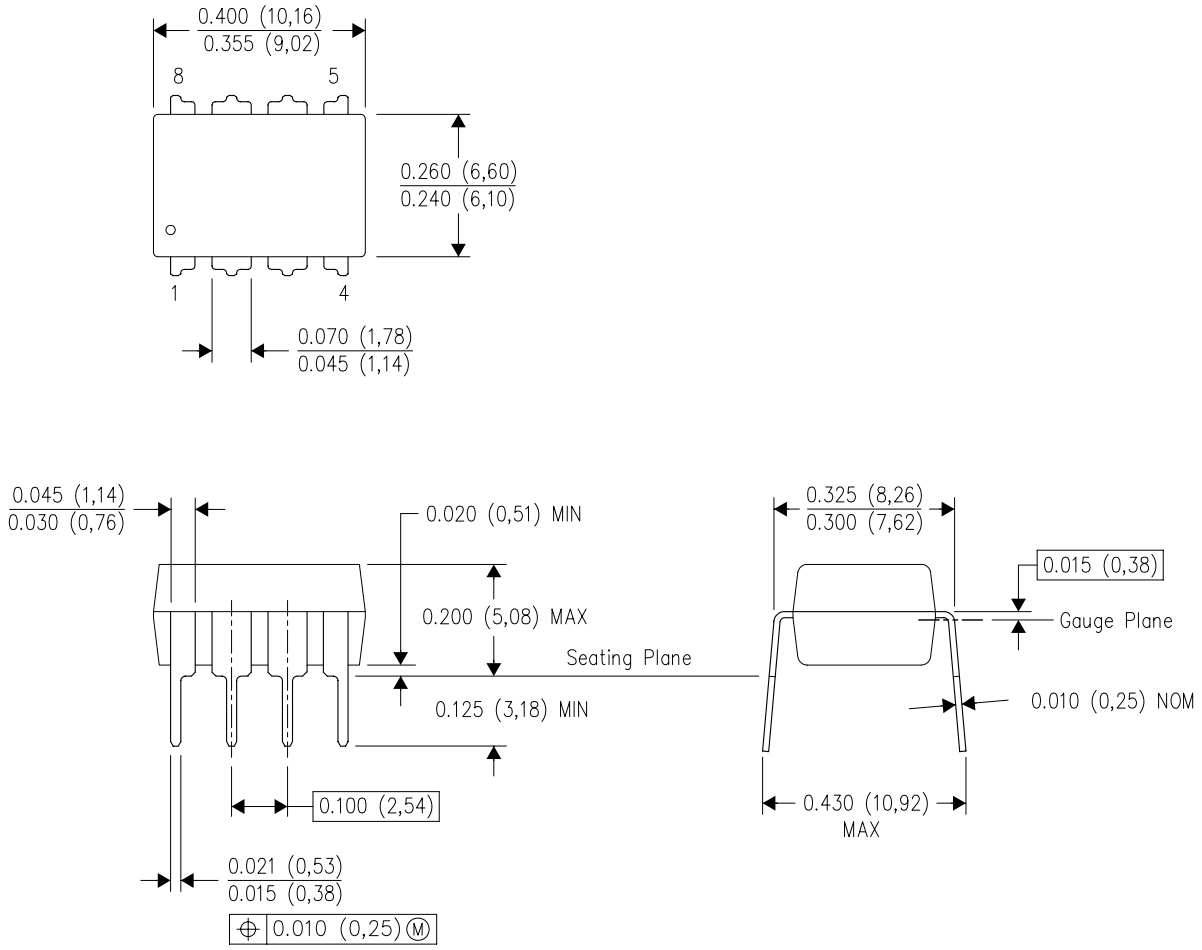
TUBE



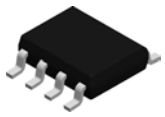
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LBC184D	D	SOIC	8	75	507	8	3940	4.32
SN65LBC184DG4	D	SOIC	8	75	507	8	3940	4.32
SN65LBC184P	P	PDIP	8	50	506	13.97	11230	4.32
SN75LBC184D	D	SOIC	8	75	507	8	3940	4.32
SN75LBC184DG4	D	SOIC	8	75	507	8	3940	4.32
SN75LBC184P	P	PDIP	8	50	506	13.97	11230	4.32

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

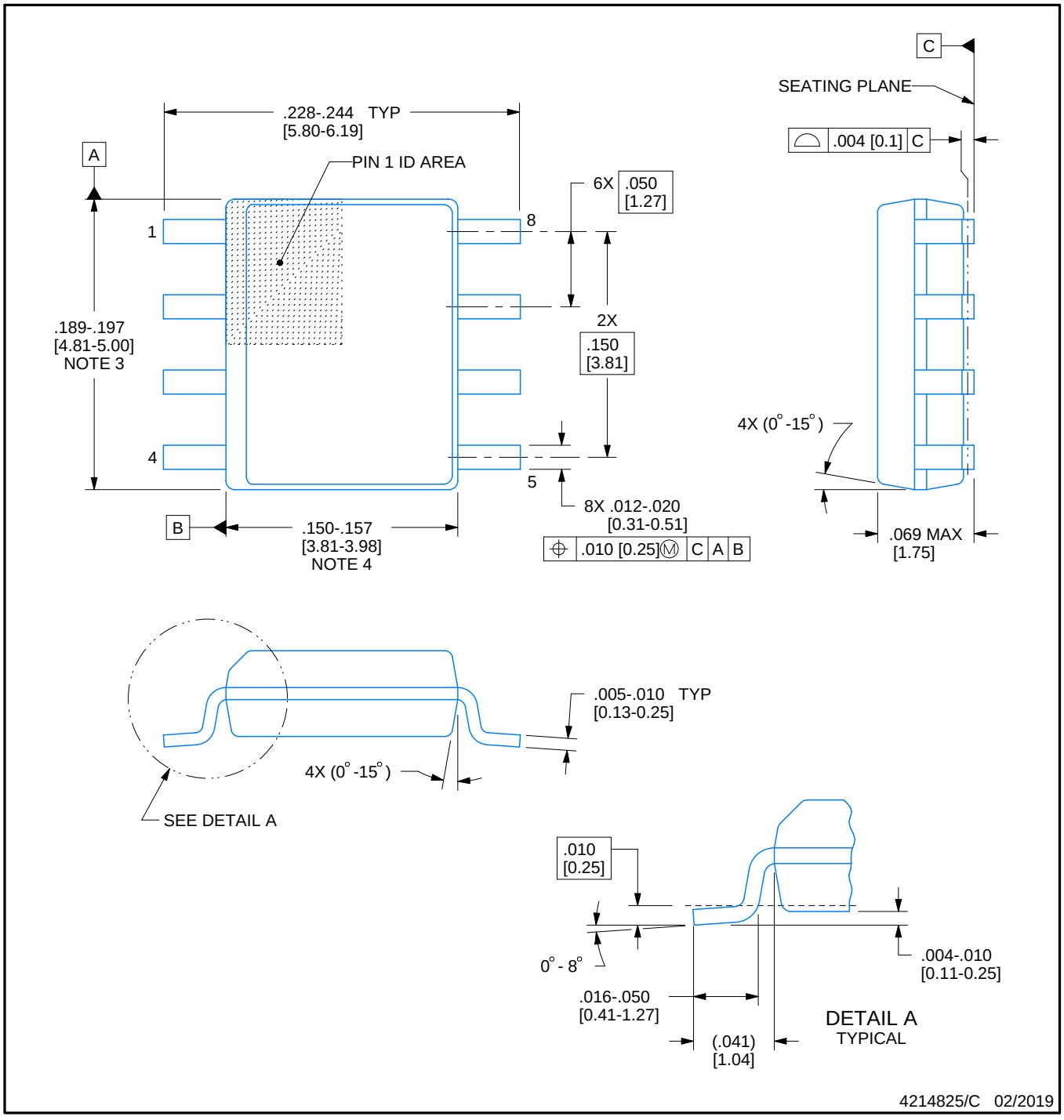


PACKAGE OUTLINE

D0008A

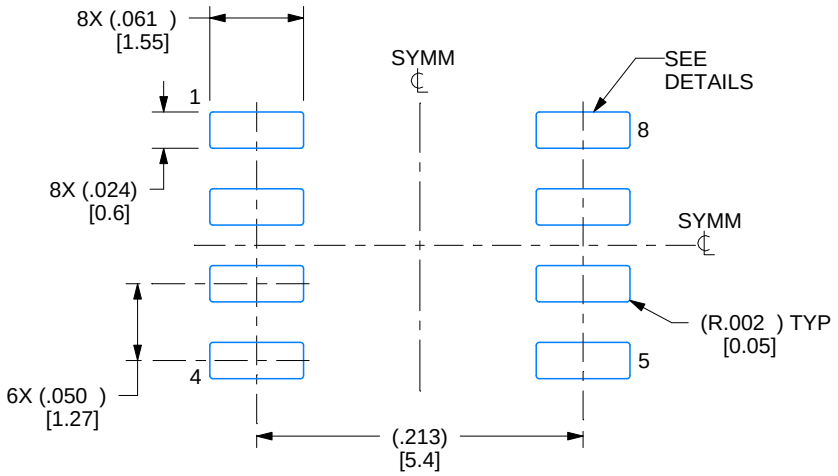
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

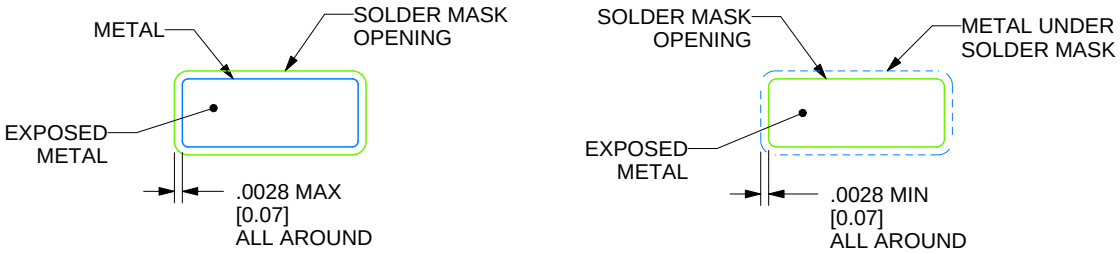


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

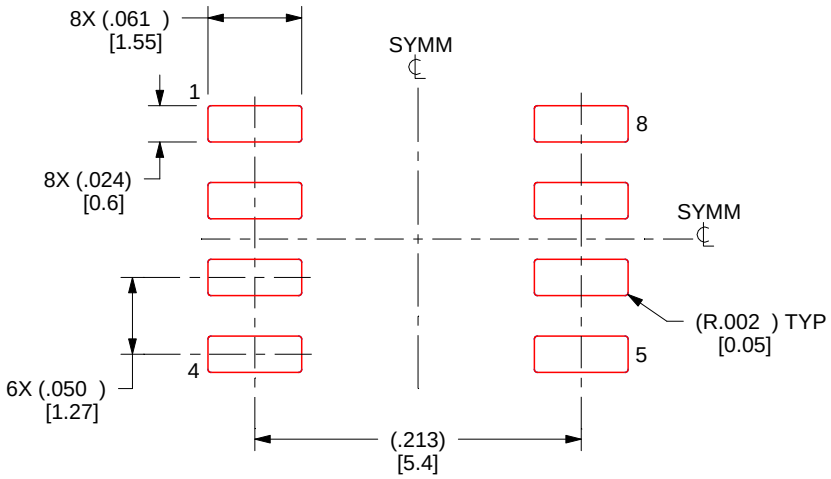
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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