THE DATASHEET OF

LMC7101BIM5X/NOPB

LMC7101, LMC7101Q-Q1 Tiny Low-Power Operational Amplifier With Rail-to-Rail Input and Output

1 Features

- Tiny 5-Pin SOT-23 Package Saves Space—Typical Circuit Layouts Take Half the Space of 8-Pin SOIC Designs
- Ensured Specifications at 2.7-V, 3-V, 5-V, 15-V Supplies
- Typical Supply Current 0.5 mA at 5 V
- Typical Total Harmonic Distortion of 0.01% at 5 V
- 1-MHz Gain Bandwidth
- Similar to Popular LMC6482 and LMC6484
- Rail-to-Rail Input and Output
- Temperature Range –40°C to 125°C (LMC7101Q-Q1)

2 Applications

- Mobile Communications
- Notebooks and PDAs
- Battery Powered Products
- Sensor Interface
- Automotive Applications (LMC7101Q-Q1)

3 Description

The LMC7101 device is a high-performance CMOS operational amplifier available in the space-saving 5-pin SOT-23 tiny package. This makes the LMC7101 ideal for space- and weight-critical designs. The performance is similar to a single amplifier of the LMC6482 and LMC6484 types, with rail-to-rail input and output, high open-loop gain, low distortion, and low-supply currents.

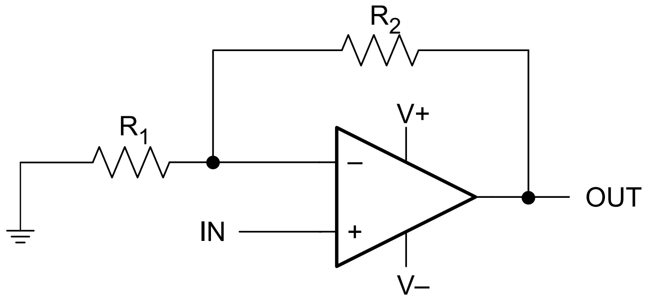
The main benefits of the tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, notebook computers, personal digital assistants, and PCMCIA cards. The tiny amplifiers can be placed on a board where they are needed, thus simplifying board layout.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMC7101, LMC7101Q-Q1	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Example Application



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4 Revision History

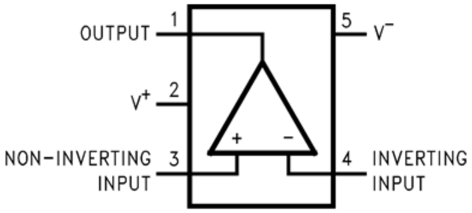
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (March 2013) to Revision G	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision E (March 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	22

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUTPUT	O	Output
2	V^+	P	Positive Supply
3	INPUT+	I	Noninverting Input
4	INPUT–	I	Inverting Input
5	V^-	P	Negative Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

	MIN	MAX	UNIT
Difference input voltage	±Supply Voltage		
Voltage at input and output pins	$(V^+) + 0.3$, $(V^-) - 0.3$		V
Supply voltage ($V^+ - V^-$)		16	V
Current at input pin	–5	5	mA
Current at output pin[3]	–35	35	mA
Current at power supply pin		35	mA
Lead temperature (soldering, 10 sec.)		260	°C
Junction temperature[4]		150	°C
Storage temperature	–65	150	°C

[1] Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
[2] If Military/Aerospace specified devices are required, contact the TI Sales Office or Distributors for availability and specifications.
[3] Applies to both single-supply and split-supply operation. Continuous short operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.
[4] The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$ and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly into a PC board.

6.2 ESD Ratings: LMC7101

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	
		Machine model (MM)	±200	

[1] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
[2] JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings: LMC7101Q-Q1

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	±1000	
		Machine model (MM)	±200	

[1] AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).[1]

		MIN	MAX	UNIT
Supply voltage, V^+		2.7	15.5	V
Junction Temperature, T_J	LMC7101AI, LMC7101BI	–40	85	°C
	LMC7101Q-Q1	–40	125	°C

[1] Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.5 Thermal Information

THERMAL METRIC[1]		LMC7101 DBV (SOT-23) 5 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	170.9	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	124.7	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	30.8	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	17.7	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	30.2	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics: 2.7 V

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 2.7 V, $V^–$ = 0 V, V_{CM} = V_O = V^+ / 2 and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS	TYP[1]	LMC7101AI		LMC7101BI		LMC7101Q-Q1[2]		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OS}	Input offset voltage average drift	V^+ = 2.7 V	0.11		6		9		9	mV
TCV_{OS}	Input offset voltage		1							μV/°C
I_B	Input bias current	–40°C ≤ T_J ≤ 125°C	1		64		64		1000	pA
I_{OS}	Input offset current	–40°C ≤ T_J ≤ 125°C	0.5		32		32		2000	pA
R_{IN}	Input resistance		>1							Tera Ω
CMRR	Common-mode rejection ratio	0 V ≤ V_{CM} ≤ 2.7 V V^+ = 2.7 V	70	55		50		50		dB
V_{CM}	Input common mode voltage range	For CMRR ≥ 50 dB	0	0		0		0		V
			3		2.7		2.7		2.7	V
PSRR	Power supply rejection ratio	V^+ = 1.35 V to 1.65 V $V^–$ = –1.35 V to –1.65 V V_{CM} = 0	60	50		45		45		dB
C_{IN}	Common-mode input capacitance		3							pF
V_O	Output swing, min	R_L = 2 kΩ	2.45	2.15		2.15		2.15		V
		R_L = 10 kΩ	2.68	2.64		2.64		2.64		
V_O	Output swing, max	R_L = 2 kΩ	0.25		0.5		0.5		0.5	V
		R_L = 10 kΩ	0.025		0.06		0.06		0.06	
I_S	Supply current		0.5		0.81		0.81		0.81	mA
		–40°C ≤ T_J ≤ 125°C	0.5		0.95		0.95		0.95	
SR	Slew rate[3]		0.7							V/μs
GBW	Gain-bandwidth product		0.6							MHz

(1) Typical values represent the most likely parametric normal.
(2) When operated at temperature between –40°C and 85°C, the LMC7101Q-Q1 will meet LMC7101BI specifications.
(3) V^+ = 15 V. Connected as a voltage follower with a 10-V step input. Number specified is the slower of the positive and negative slew rates. R_L = 100 kΩ connected to 7.5 V. Amplifier excited with 1 kHz to produce V_O = 10 V_{PP}.

6.7 DC Electrical Characteristics: 3 V

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 3 V, V^- = 0 V, V_{CM} = 1.5 V, V_O = V^+ / 2 and R_L = 1 MΩ.

PARAMETER		TEST CONDITIONS	TYP(1)	LMC7101AI		LMC7101BI		LMC7101Q-Q1(2)		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OS}	Input offset voltage				4		7		7	mV
		–40°C ≤ T_J ≤ 125°C	0.11		6		9			
TCV_{OS}	Input offset voltage average drift		1							µV/°C
I_B	Input current	–40°C ≤ T_J ≤ 125°C	1		64		64		1000	pA
I_{OS}	Input offset current	–40°C ≤ T_J ≤ 125°C	0.5		32		32		2000	pA
R_{IN}	Input resistance		>1							Tera Ω
CMRR	Common-mode rejection ratio	0 V ≤ V_{CM} ≤ 3 V V^+ = 3 V	74	64		60		60		db
V_{CM}	Input common-mode voltage range	For CMRR ≥ 50 dB	0	0		0		0		V
			3.3		3		3		3	
PSRR	Power supply rejection ratio	V^+ = 1.5 V to 7.5 V V^- = –1.5 V to –7.5 V V_O = V_{CM} = 0	80	68		60		60		dB
C_{IN}	Common-mode input capacitance		3							pF
V_O	Output swing, min	R_L = 2 kΩ	2.8	2.6		2.6		2.6		V
		R_L = 600 Ω	0.2		0.4		0.4		0.4	
V_O	Output swing, max	R_L = 2 kΩ	2.7	2.5		2.5		2.5		V
		R_L = 600 Ω	0.37		0.6		0.6		0.6	
I_S	Supply current				0.81		0.81		0.81	mA
		–40°C ≤ T_J ≤ 125°C	0.5		0.95		0.95		0.95	

(1) Typical values represent the most likely parametric normal.

(2) When operated at temperature between –40°C and 85°C, the LMC7101Q-Q1 will meet LMC7101BI specifications.

6.8 DC Electrical Characteristics: 5 V

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = 1.5 V, V_O = V^+/ 2 and R_L = 1 MΩ.

PARAMETER		TEST CONDITIONS		TYP[1]	LMC7101AI		LMC7101BI		LMC7101Q-Q1[2]		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
V_{OS}	Input offset voltage	V^+ = 5 V		0.11		3		7		7	mV
		V^+ = 5 V, –40°C ≤ T_J ≤ 125°C		0.11		5		9		9	
TCV_{OS}	Input offset voltage average drift			1							μV/°C
I_B	Input current	–40°C ≤ T_J ≤ 125°C		1		64		64		1000	pA
I_{OS}	Input offset current	–40°C ≤ T_J ≤ 125°C		0.5		32		32		2000	pA
R_{IN}	Input resistance			>1							Tera Ω
CMRR	Common-mode rejection ratio	0 V ≤ V_{CM} ≤ 5 V LMC7101Q-Q1 at 125°C 0.2 V ≤ V_{CM} ≤ 4.8 V		82	65		60		60		db
		0 V ≤ V_{CM} ≤ 5 V LMC7101Q-Q1 at 125°C 0.2 V ≤ V_{CM} ≤ 4.8 V –40°C ≤ T_J ≤ 125°C		82	60		55		55		
+PSRR	Positive power supply rejection ratio	V^+ = 5 V to 15 V V^- = 0 V, V_O = 1.5 V		82	70		65		65		dB
		V^+ = 5 V to 15 V V^- = 0 V, V_O = 1.5 V –40°C ≤ T_J ≤ 125°C		82	65		62		62		
–PSRR	Negative power supply rejection ratio	V^- = –5 V to –15 V V^+ = 0 V, V_O = –1.5 V		82	70		65		65		dB
		V^- = –5 V to –15 V V^+ = 0 V, V_O = –1.5 V –40°C ≤ T_J ≤ 125°C		82	65		62		62		
V_{CM}	Input common-mode voltage range	For CMRR ≥ 50 dB		–0.3	–0.2		–0.2		–0.2		V
		For CMRR ≥ 50 dB –40°C ≤ T_J ≤ 125°C		–0.3	0		0		0.2		
				5.3		5.2		5.2		5.2	V
		–40°C ≤ T_J ≤ 125°C		5.3		5		5		4.8	
C_{IN}	Common-mode input capacitance			3							pF
V_O	Output swing	R_L = 2 kΩ		4.9	4.7		4.7		4.7		V
		R_L = 2 kΩ, –40°C ≤ T_J ≤ 125°C		4.9	4.6		4.6		4.54		
				0.1		0.18		0.18		0.18	V
		–40°C ≤ T_J ≤ 125°C		0.1		0.24		0.24		0.28	
		R_L = 600 Ω		4.7	4.5		4.5		4.5		V
		R_L = 600 Ω, –40°C ≤ T_J ≤ 125°C		4.7	4.24		4.24		4.28		
				0.3		0.5		0.5		0.5	V
		–40°C ≤ T_J ≤ 125°C		0.3		0.65		0.65		0.8	
I_{SC}	Output short circuit current	Sourcing	V_O = 0 V 24	24	16		16		16		mA
			V_O = 0 V 24 –40°C ≤ T_J ≤ 125°C	24	11		11		9		
		Sinking	V_O = 5 V	19	11		11		11		mA
			V_O = 5 V –40°C ≤ T_J ≤ 125°C	19	7.5		7.5		5.8		
I_S	Supply current			0.5		0.85		0.85		0.85	mA
		–40°C ≤ T_J ≤ 125°C		0.5		1		1		1	

(1) Typical values represent the most likely parametric normal.
(2) When operated at temperature between –40°C and 85°C, the LMC7101Q-Q1 will meet LMC7101BI specifications.

6.9 DC Electrical Characteristics: 15 V

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 15 V, V^- = 0 V, V_{CM} = 1.5 V, V_O = V^+ / 2 and R_L = 1 MΩ.

PARAMETER		TEST CONDITIONS		TYP(1)	LMC7101AI		LMC7101BI		LMC7101Q-Q1(2)		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
V_{OS}	Input offset voltage			0.11							mV
TCV_{OS}	Input offset voltage average drift			1							µV/°C
I_B	Input current	–40°C ≤ T_J ≤ 125°C		1		64		64		1000	pA
I_{OS}	Input offset current	–40°C ≤ T_J ≤ 125°C		0.5		32		32		2000	pA
R_{IN}	Input resistance			>1							Tera Ω
CMRR	Common-mode rejection ratio	0 V ≤ V_{CM} ≤ 15 V LMC7101Q-Q1 at 125°C 0.2 V ≤ V_{CM} ≤ 14.8 V		82	70		65		65		dB
		0 V ≤ V_{CM} ≤ 15 V LMC7101Q-Q1 at 125°C 0.2 V ≤ V_{CM} ≤ 14.8 V –40°C ≤ T_J ≤ 125°C		82	65		60		60		
+PSRR	Positive power supply rejection ratio	V^+ = 5 V to 15 V V^- = 0 V, V_O = 1.5 V		82	70		65		65		dB
		V^+ = 5 V to 15 V V^- = 0 V, V_O = 1.5 V –40°C ≤ T_J ≤ 125°C		82	65		62		62		
–PSRR	Negative power supply rejection ratio	V^- = –5 V to –15 V V^+ = 0 V, V_O = –1.5 V		82	70		65		65		dB
		V^- = –5 V to –15 V V^+ = 0 V, V_O = –1.5 V –40°C ≤ T_J ≤ 125°C		82	65		62		62		
V_{CM}	Input common-mode voltage range	V^+ = 5 V For CMRR ≥ 50 dB		–0.3	–0.2		–0.2		–0.2		V
		V^+ = 5 V For CMRR ≥ 50 dB –40°C ≤ T_J ≤ 125°C		-0.3	0		0		0.2		
				15.3		15.2		15.2		15.2	V max
		–40°C ≤ T_J ≤ 125°C		15.3		15		15		14.8	
A_V	Large signal voltage gain(3)	Sourcing	R_L = 2 kΩ	340	80		80		80		V/mV
			R_L = 2 kΩ –40°C ≤ T_J ≤ 125°C	340	40		40		30		
		Sinking	R_L = 2 kΩ	24	15		15		15		
			R_L = 2 kΩ –40°C ≤ T_J ≤ 125°C	24	10		10		4		
		Sourcing	R_L = 600 Ω	300	34		34		34		V/mV
		Sinking		15	6		6		6		
C_{IN}	Input capacitance			3							pF
V_O	Output swing	V^+ = 15 V R_L = 2 kΩ		14.7	14.4		14.4		14.4		V
		V^+ = 15 V R_L = 2 kΩ –40°C ≤ T_J ≤ 125°C		14.7	14.2		14.2		14.2		
				0.16		0.32		0.32		0.32	V
		–40°C ≤ T_J ≤ 125°C		0.16		0.45		0.45		0.45	
		V^+ = 15 V R_L = 600 Ω		14.1	13.4		13.4		13.4		V
		V^+ = 15 V R_L = 600 Ω –40°C ≤ T_J ≤ 125°C		14.1	13		13		12.85		
				0.5		1		1		1	V
		–40°C ≤ T_J ≤ 125°C		0.5		1.3		1.3		1.5	

(1) Typical values represent the most likely parametric normal.
(2) When operated at temperature between –40°C and 85°C, the LMC7101Q-Q1 will meet LMC7101BI specifications.
(3) V^+ = 15 V, V_{CM} = 1.5 V and R_L connect to 7.5 V. For sourcing tests, 7.5 V ≤ V_O ≤ 12.5 V. For sinking tests, 2.5 V ≤ V_O ≤ 7.5 V.

DC Electrical Characteristics: 15 V (continued)

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 15 V, V^- = 0 V, V_{CM} = 1.5 V, V_O = V^+ / 2 and R_L = 1 MΩ.

PARAMETER		TEST CONDITIONS		TYP(1)	LMC7101AI		LMC7101BI		LMC7101Q-Q1(2)		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
I_{SC}	Output short circuit current(4)	Sourcing	V_O = 0 V	50	30		30		30		mA
			V_O = 0 V –40°C ≤ T_J ≤ 125°C	50	20		20		20		
		Sinking	V_O = 12 V	50	30		30		30		
			V_O = 12 V –40°C ≤ T_J ≤ 125°C	50	20		20		20		
I_S	Supply current			0.8		1.5		1.5		1.5	mA
		–40°C ≤ T_J ≤ 125°C				1.71		1.71		1.75	

(4) Do not short circuit output to V^+ when V^+ is greater than 12 V or reliability will be adversely affected.

6.10 AC Electrical Characteristics: 5 V

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = 1.5 V, V_O = V^+ / 2 and R_L = 1 MΩ.

PARAMETER		TEST CONDITIONS	TYP(1)	LMC7101AI LIMIT(2)	LMC7101BI LIMIT(2)	UNIT
THD	Total harmonic distortion	f = 10 kHz, A_V = –2 R_L = 10 kΩ, V_O = 4 V_{PP}	0.01%			
SR	Slew rate		1			V/µs
GBW	Gain bandwidth product		1			MHz

(1) Typical values represent the most likely parametric normal.
(2) All limits are specified by testing or statistical analysis.

6.11 AC Electrical Characteristics: 15 V

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 15 V, V^- = 0 V, V_{CM} = 1.5 V, V_O = V^+ / 2 and R_L = 1 MΩ.

PARAMETER		TEST CONDITIONS	TYP(1)	LMC7101AI		LMC7101BI		LMC7101Q-Q1(2)		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
SR	Slew rate(3)	V^+ = 15 V	1.1	0.5		0.5		0.5		V/µs min
		V^+ = 15 V, –40°C ≤ T_J ≤ 125°C		0.4		0.4		0.4		
GBW	Gain-bandwidth product	V^+ = 15 V	1.1							MHz
φ_m	Phase margin		45							deg
G_m	Gain margin		10							dB
e_n	Input-referred voltage noise	f = 1 kHz, V_{CM} = 1 V	37							$\frac{nV}{\sqrt{Hz}}$
I_n	Input-referred current noise	f = 1 kHz	1.5							$\frac{fA}{\sqrt{Hz}}$
THD	Total harmonic distortion	f = 10 kHz, A_V = –2 R_L = 10 kΩ V_O = 8.5 V_{PP}	0.01%							

(1) Typical values represent the most likely parametric normal.
(2) When operated at temperature between –40°C and 85°C, the LMC7101Q-Q1 will meet LMC7101BI specifications.
(3) V^+ = 15 V. Connected as a voltage follower with a 10-V step input. Number specified is the slower of the positive and negative slew rates. R_L = 100 kΩ connected to 7.5 V. Amplifier excited with 1 kHz to produce V_O = 10 V_{PP}.

6.12 Typical Characteristics

6.12.1 Typical Characteristics: 2.7 V

$V^+ = 2.7$ V, $V^- = 0$ V, $T_A = 25°C$, unless otherwise specified.

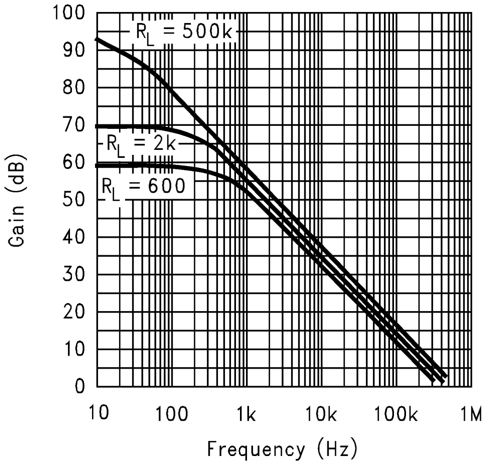


Figure 1. Open Loop Frequency Response

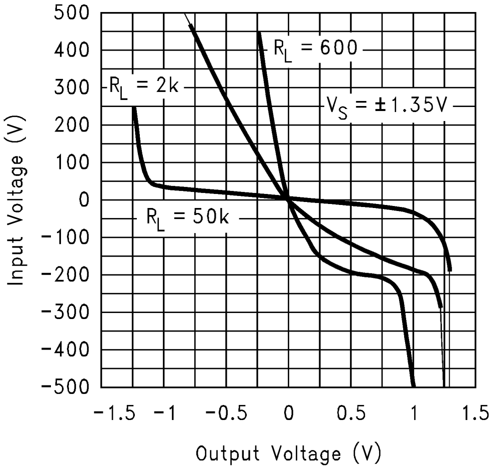


Figure 2. Input Voltage vs Output Voltage

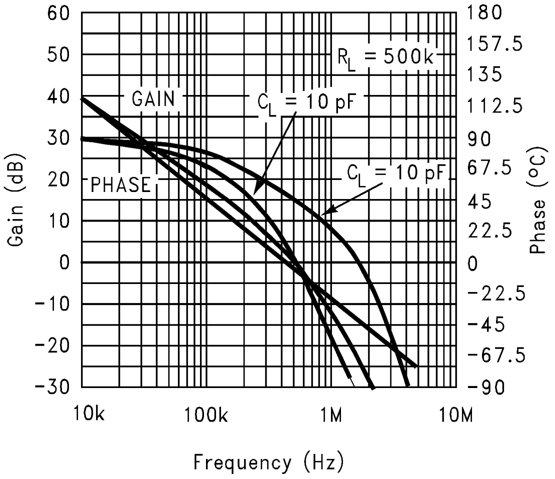


Figure 3. Gain and Phase vs Capacitance Load

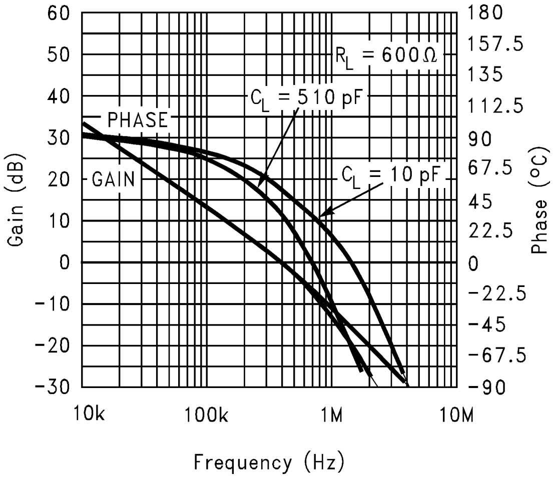


Figure 4. Gain and Phase vs Capacitance Load

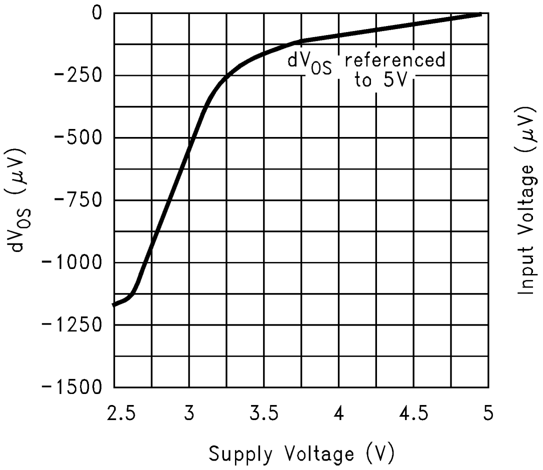


Figure 5. dV_{OS} vs Supply Voltage

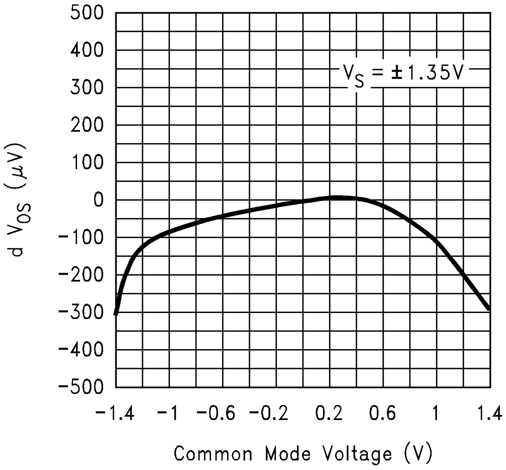


Figure 6. dV_{OS} vs Common Mode Voltage

Typical Characteristics: 2.7 V (continued)

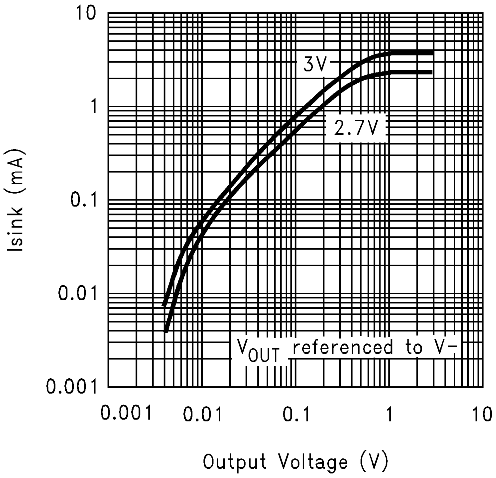


Figure 7. Sinking Current vs Output Voltage

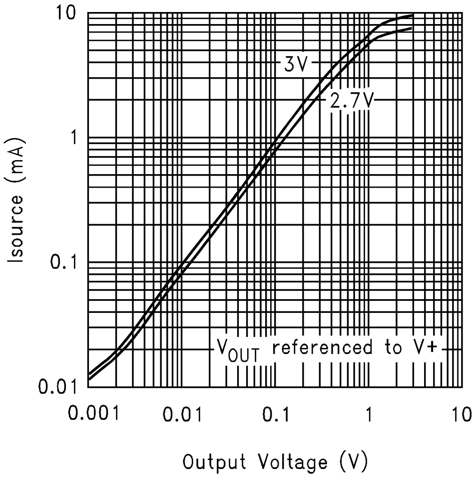


Figure 8. Sourcing Current vs Output Voltage

6.12.2 Typical Characteristics: 3 V

$V^+ = 3$ V, $V^- = 0$ V, $T_A = 25°C$, unless otherwise specified.

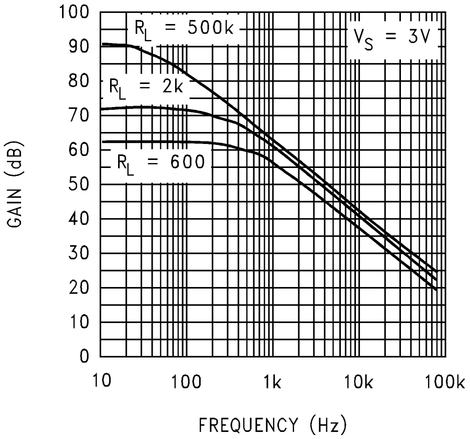


Figure 9. Open Loop Frequency Response

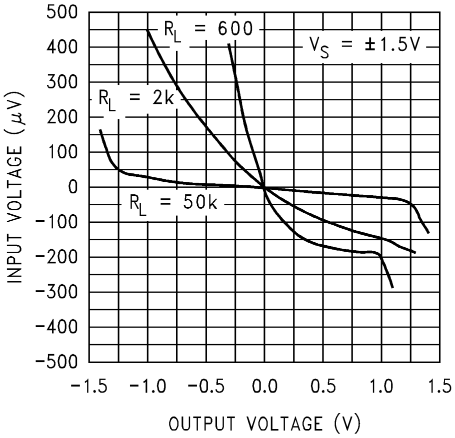


Figure 10. Input Voltage vs Output Voltage

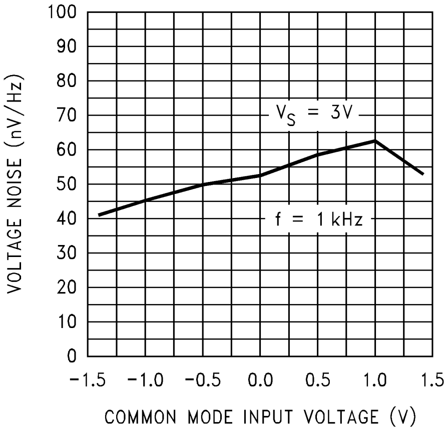


Figure 11. Input Voltage Noise vs Input Voltage

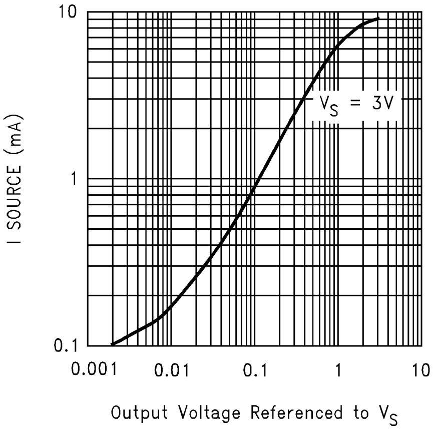


Figure 12. Sourcing Current vs Output Voltage

Typical Characteristics: 3 V (continued)

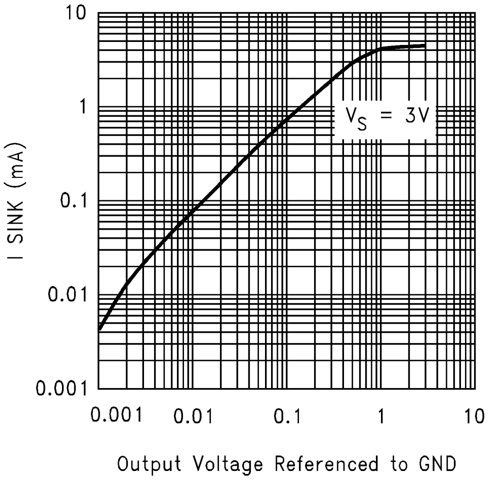


Figure 13. Sinking Current vs Output Voltage

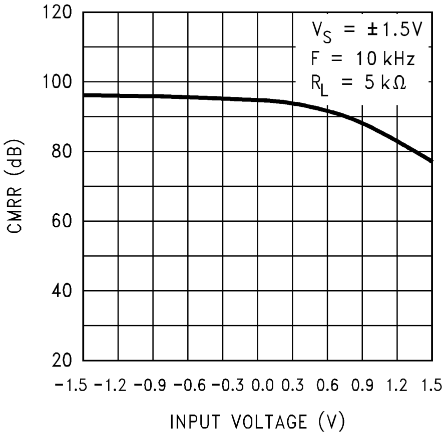


Figure 14. CMRR vs Input Voltage

6.12.3 Typical Characteristics: 5 V

$V^+ = 5$ V, $V^- = 0$ V, $T_A = 25°C$, unless otherwise specified.

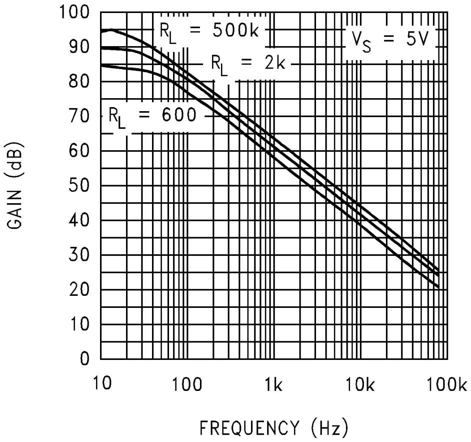


Figure 15. Open Loop Frequency Response

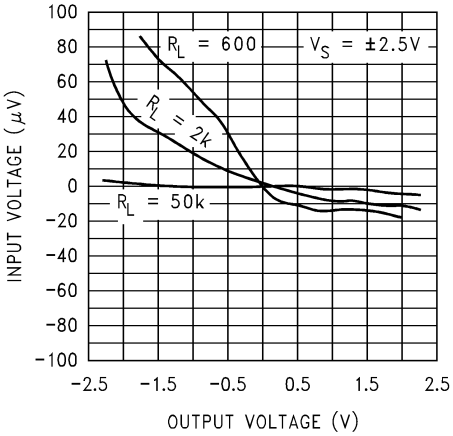


Figure 16. Input Voltage vs Output Voltage

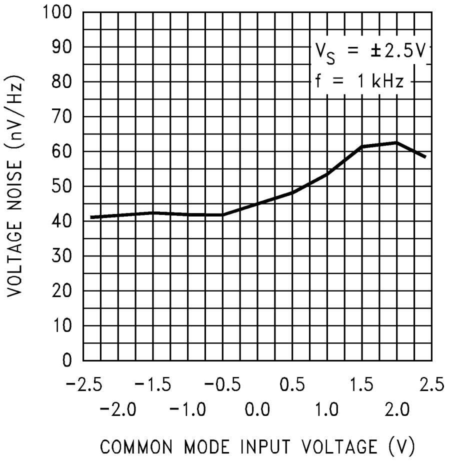


Figure 17. Input Voltage Noise vs Input Voltage

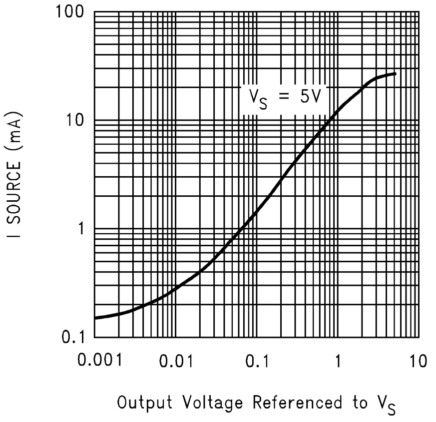


Figure 18. Sourcing Current vs Output Voltage

Typical Characteristics: 5 V (continued)

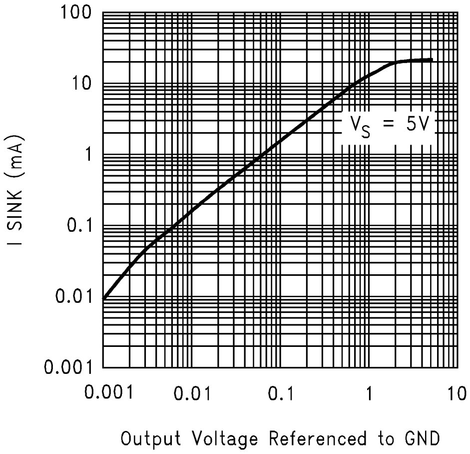


Figure 19. Sinking Current vs Output Voltage

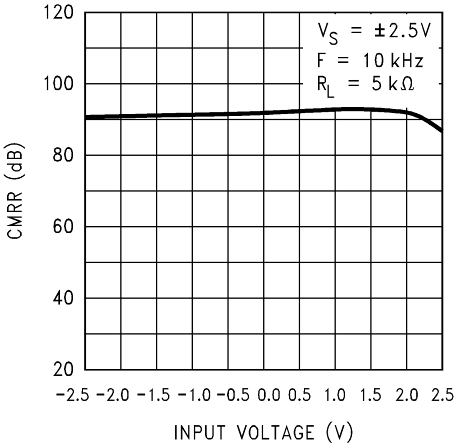


Figure 20. CMRR vs Input Voltage

6.12.4 Typical Characteristics: 15 V

V^+ = +15 V, V^- = 0 V, T_A = 25°C, unless otherwise specified.

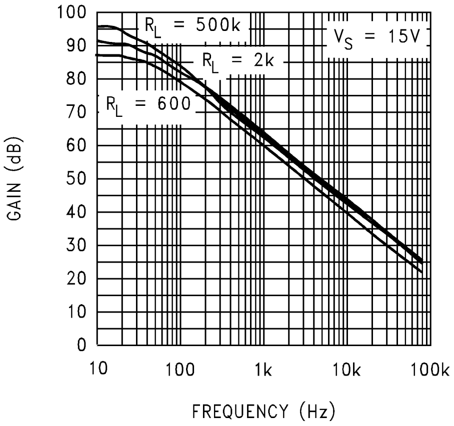


Figure 21. Open Loop Frequency Response

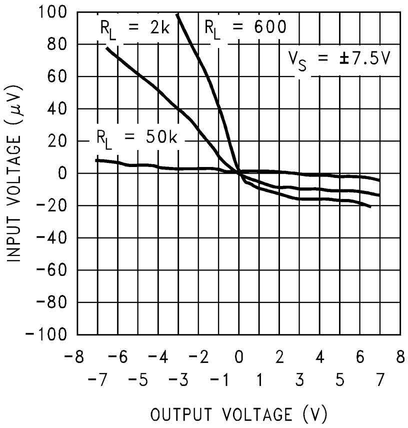


Figure 22. Input Voltage vs Output Voltage

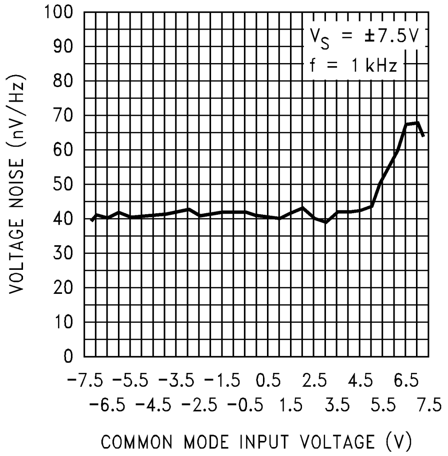


Figure 23. Input Voltage Noise vs Input Voltage

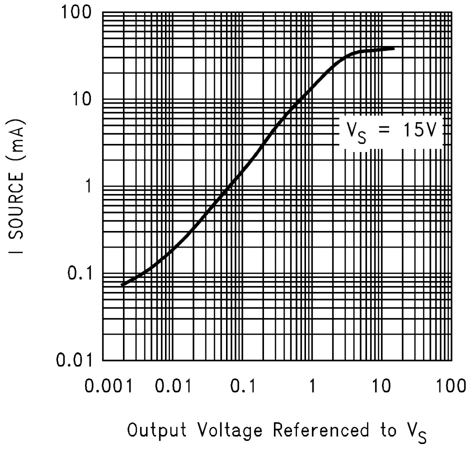


Figure 24. Sourcing Current vs Output Voltage

Typical Characteristics: 15 V (continued)

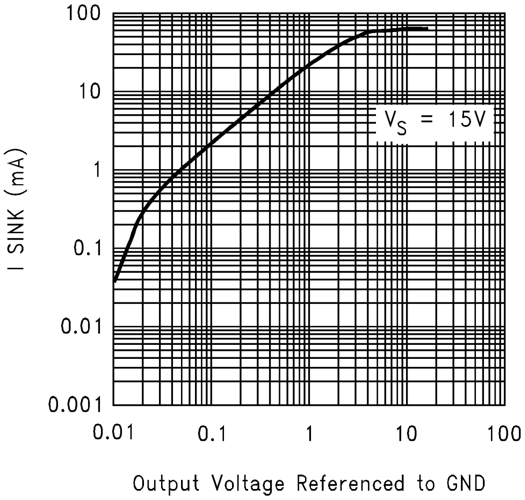


Figure 25. Sinking Current vs Output Voltage

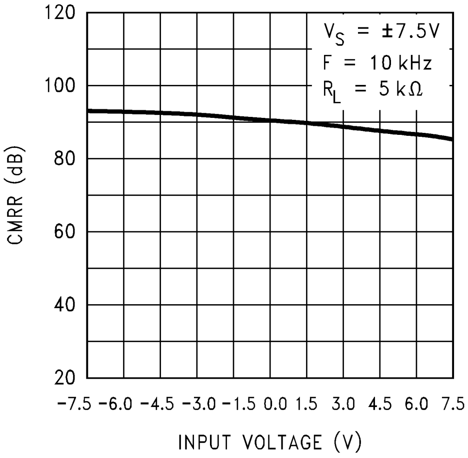


Figure 26. CMRR vs Input Voltage

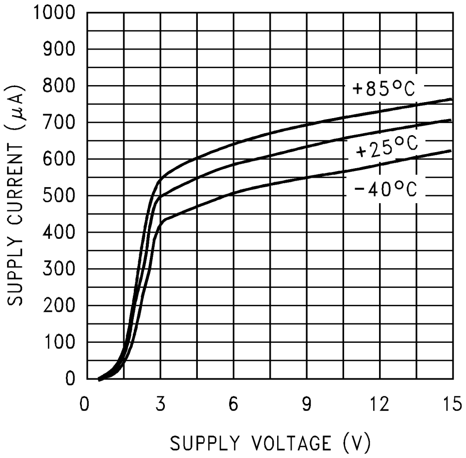


Figure 27. Supply Current vs Supply Voltage

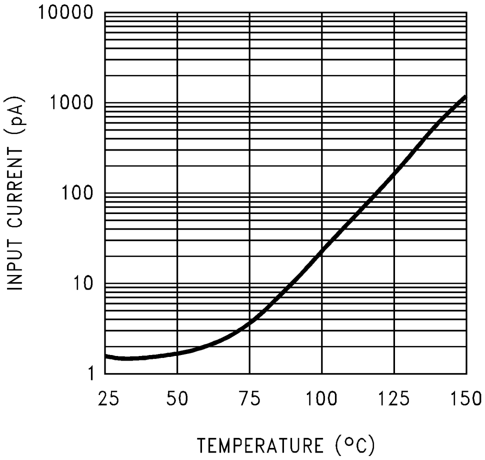


Figure 28. Input Current vs Temperature

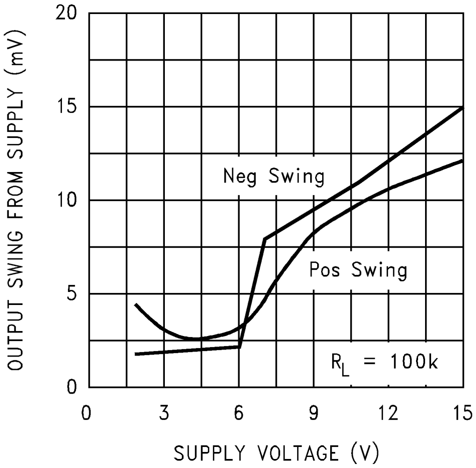


Figure 29. Output Voltage Swing vs Supply Voltage

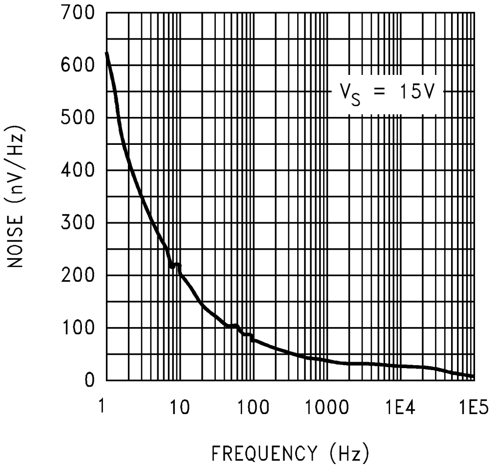


Figure 30. Input Voltage Noise vs Frequency

Typical Characteristics: 15 V (continued)

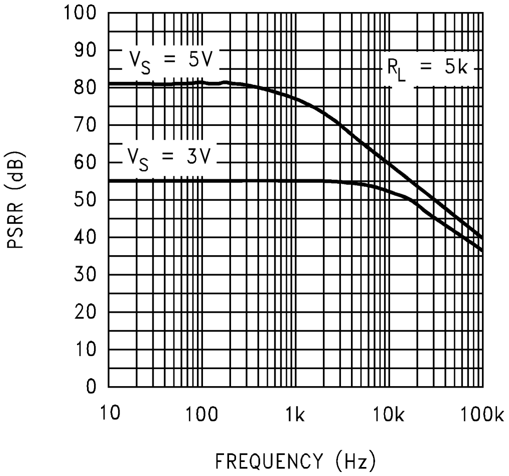


Figure 31. Positive PSRR vs Frequency

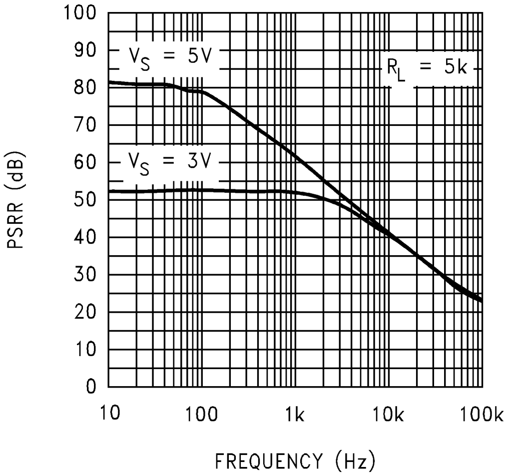


Figure 32. Negative PSRR vs Frequency

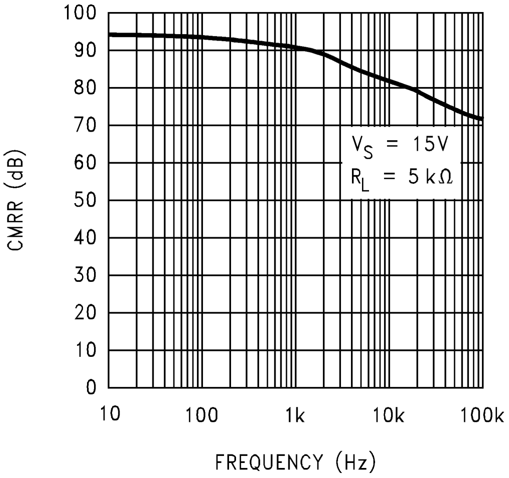


Figure 33. CMRR vs Frequency

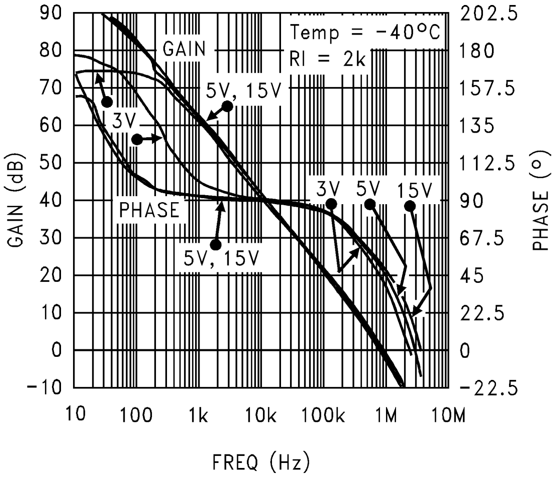


Figure 34. Open Loop Frequency Response at –40°C

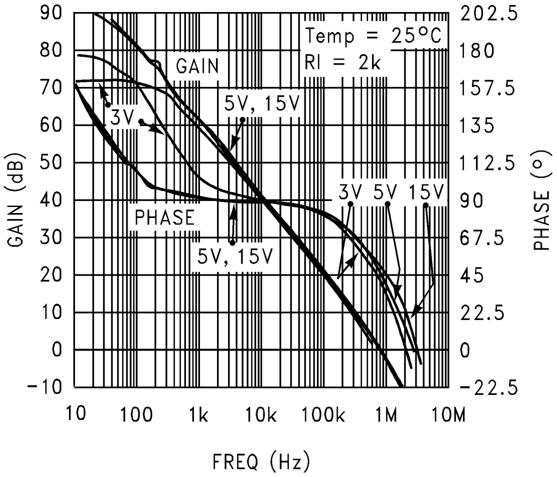


Figure 35. Open Loop Frequency Response at 25°C

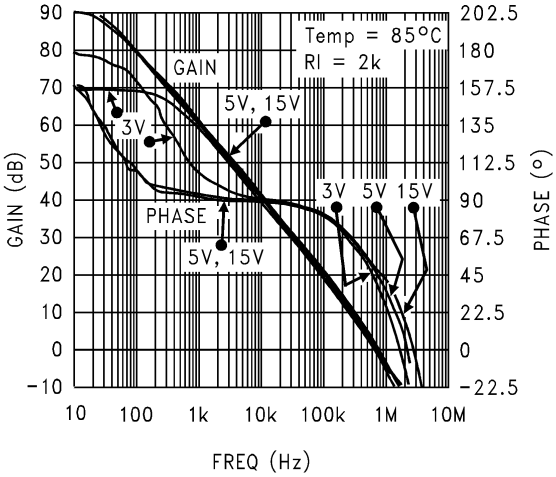


Figure 36. Open Loop Frequency Response at 85°C

Typical Characteristics: 15 V (continued)

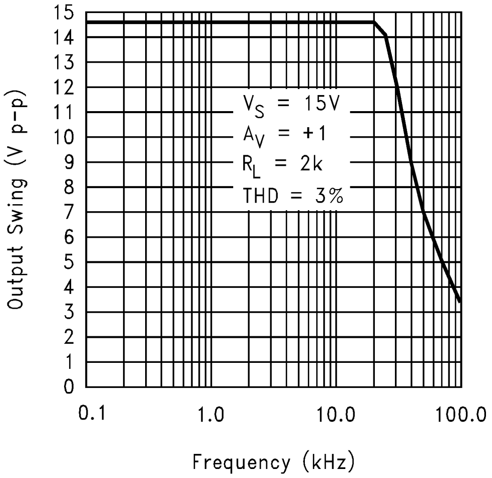


Figure 37. Maximum Output Swing vs Frequency

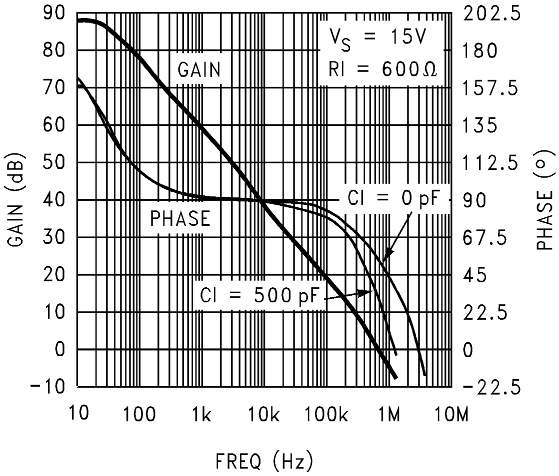


Figure 38. Gain and Phase vs Capacitive Load

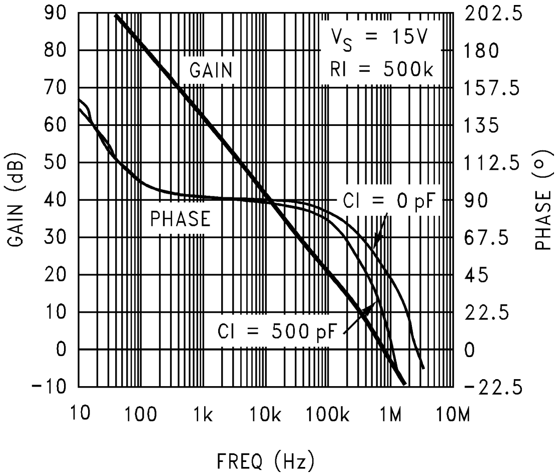


Figure 39. Gain and Phase vs Capacitive Load

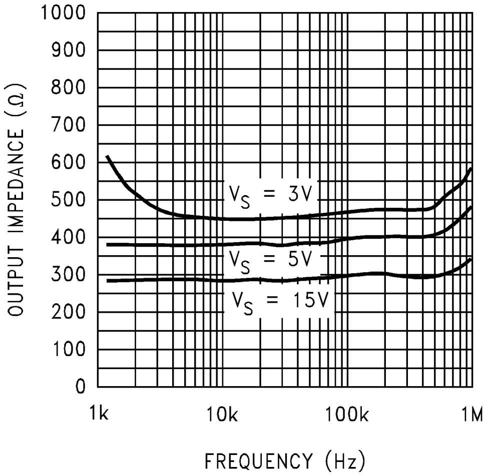


Figure 40. Output Impedance vs Frequency

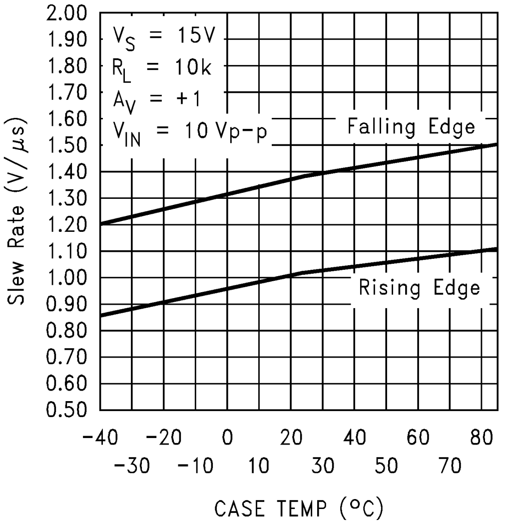


Figure 41. Slew Rate vs Temperature

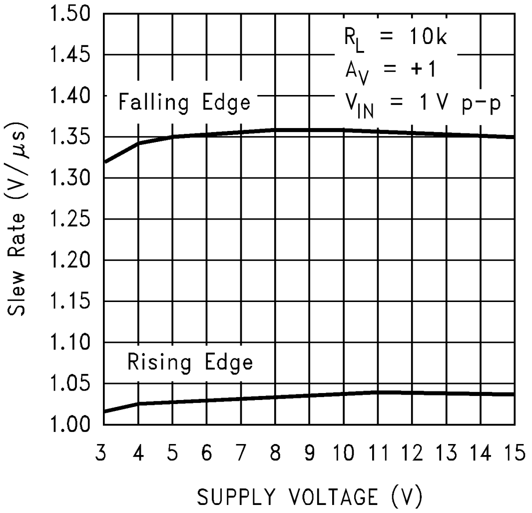


Figure 42. Slew Rate vs Supply Voltage

Typical Characteristics: 15 V (continued)

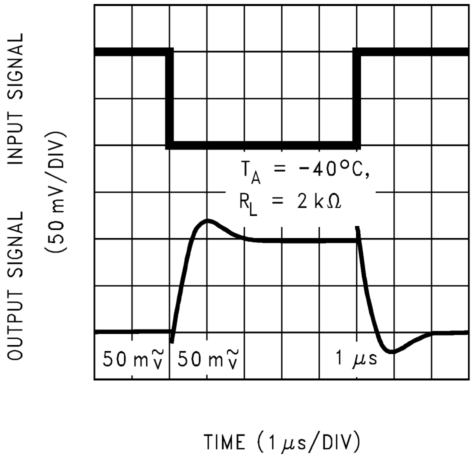


Figure 43. Inverting Small Signal Pulse Response

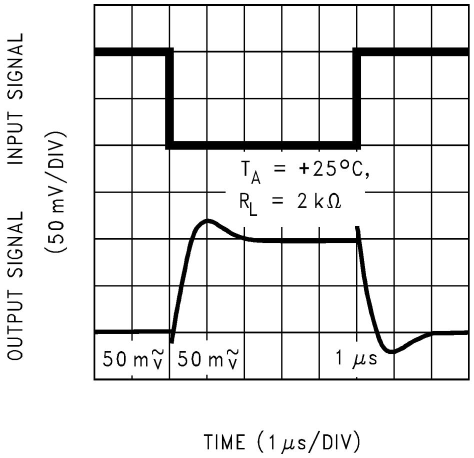


Figure 44. Inverting Small Signal Pulse Response

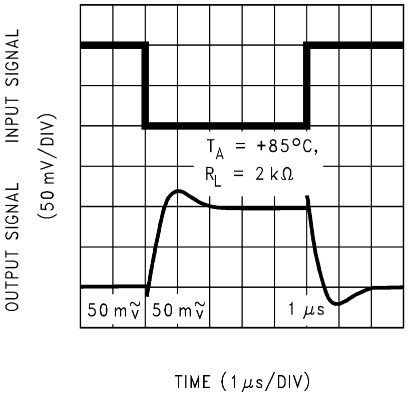


Figure 45. Inverting Small Signal Pulse Response

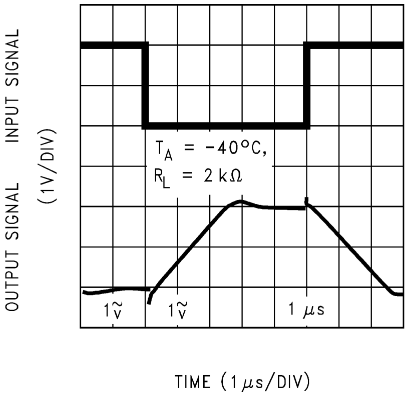


Figure 46. Inverting Large Signal Pulse Response

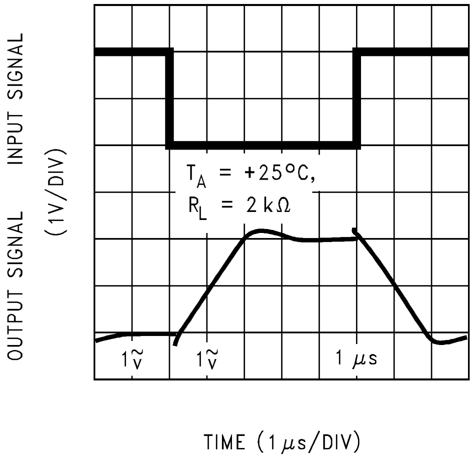


Figure 47. Inverting Large Signal Pulse Response

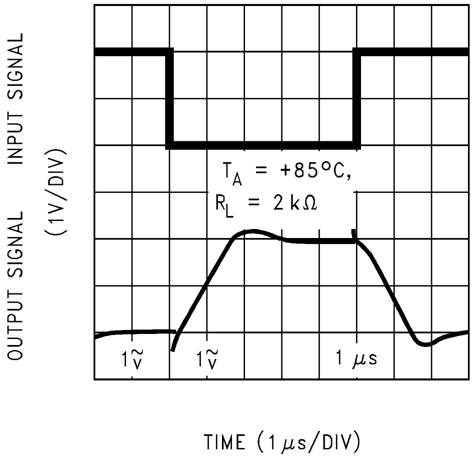


Figure 48. Inverting Large Signal Pulse Response

Typical Characteristics: 15 V (continued)

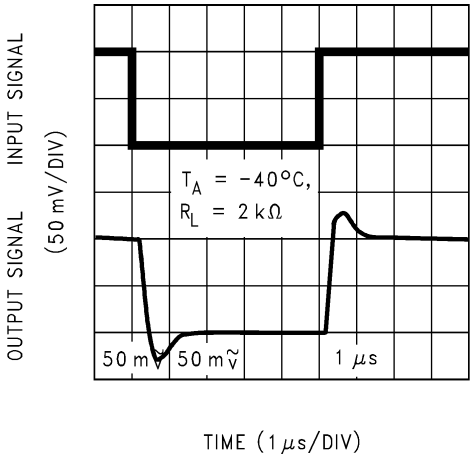


Figure 49. Noninverting Small Signal Pulse Response

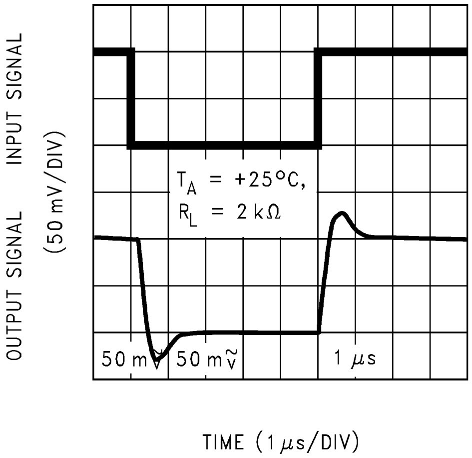


Figure 50. Noninverting Small Signal Pulse Response

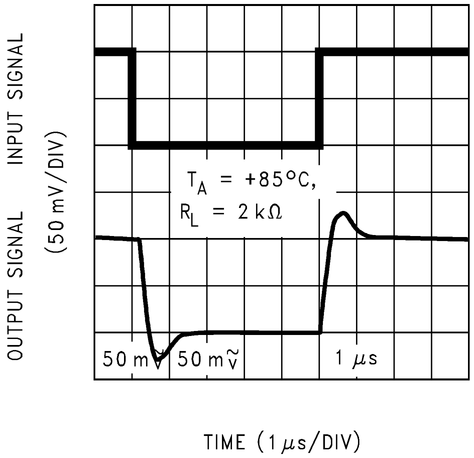


Figure 51. Noninverting Small Signal Pulse Response

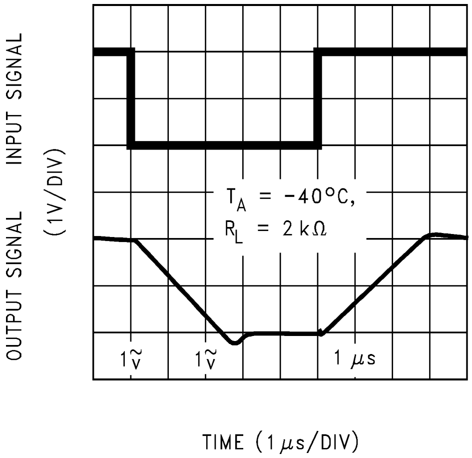


Figure 52. Noninverting Large Signal Pulse Response

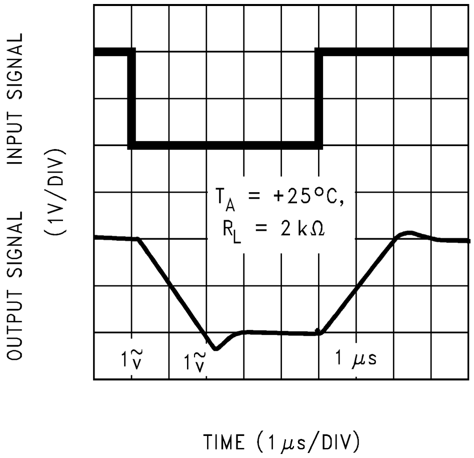


Figure 53. Noninverting Large Signal Pulse Response

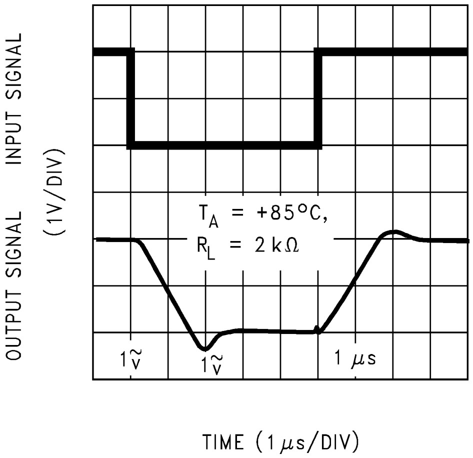


Figure 54. Noninverting Large Signal Pulse Response

Typical Characteristics: 15 V (continued)

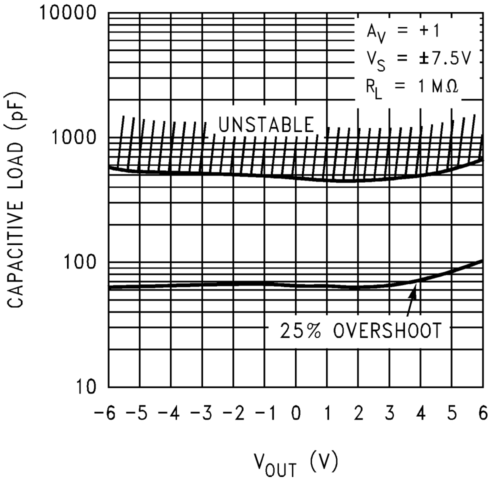


Figure 55. Stability vs Capacitive Load

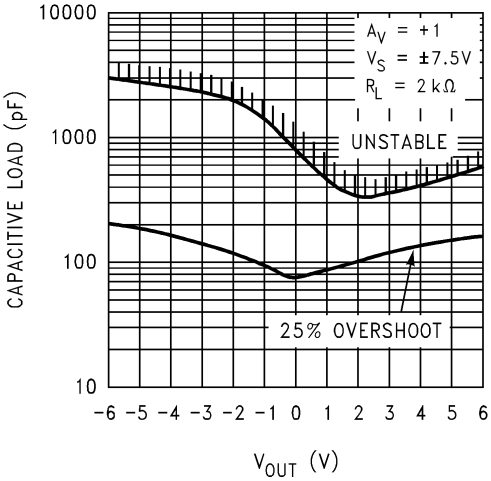


Figure 56. Stability vs Capacitive Load

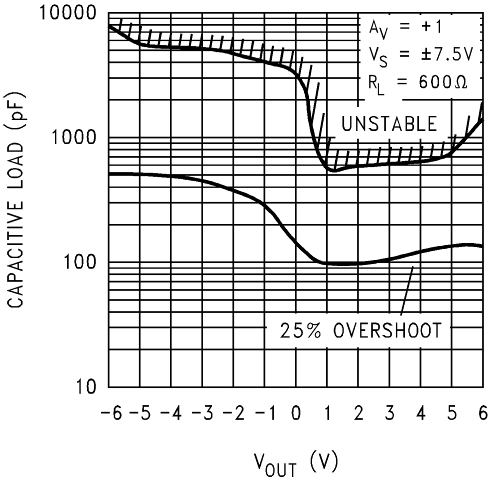


Figure 57. Stability vs Capacitive Load

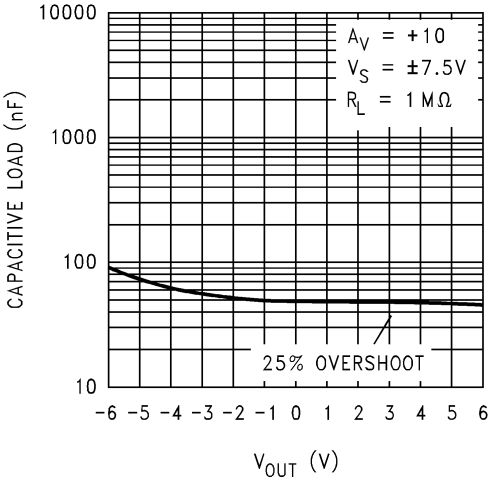


Figure 58. Stability vs Capacitive Load

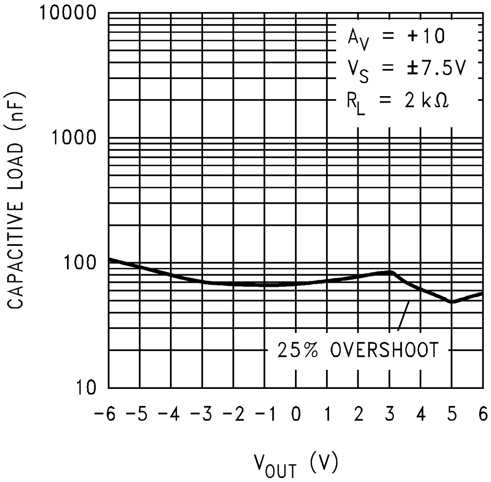


Figure 59. Stability vs Capacitive Load

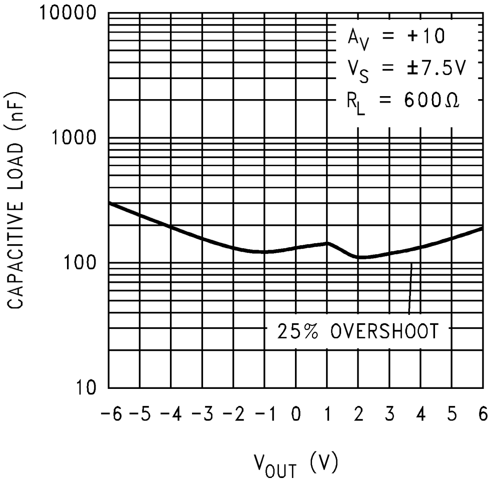


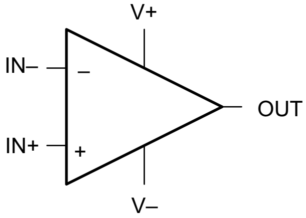
Figure 60. Stability vs Capacitive Load

7 Detailed Description

7.1 Overview

The LMC7101 is a single channel, low-power operational amplifier available in a space-saving SOT-23 package, offering rail-to-rail input and output operation across a wide range of power supply configurations. The LMC7101Q-Q1 is the automotive Q-grade variant.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Benefits of the LMC7101 Tiny Amplifier

7.3.1.1 Size

The small footprint of the SOT-23-5 packaged tiny amplifier, (0.12 × 0.118 inches, 3.05 × 3 mm) saves space on printed circuit boards, and enable the design of smaller electronic products. Because they are easier to carry, many customers prefer smaller and lighter products.

7.3.1.2 Height

The 0.056 inches (1.43 mm) height of the tiny amplifier makes is suitable for use in a wide range of portable applications in which a thin profile is required.

7.3.1.3 Signal Integrity

Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the tiny amplifier can be placed closer to the signal source, thus reducing noise pickup and increasing signal integrity. The tiny amplifier can also be placed next to the signal destination, such as a buffer, for the reference of an analog-to-digital converter.

7.3.1.4 Simplified Board Layout

The tiny amplifier can simplify board layout in several ways. Avoid long PCB traces by correctly placing amplifiers instead of routing signals to a dual or quad device.

By using multiple tiny amplifiers instead of duals or quads, complex signal routing and possibly crosstalk can be reduced.

7.3.1.5 Low THD

The high open-loop gain of the LMC7101 amp allows it to achieve very low audio distortion—typically 0.01% at 10 kHz with a 10-kΩ load at 5-V supplies. This makes the tiny amplifier an excellent for audio, modems, and low frequency signal processing.

7.3.1.6 Low Supply Current

The typical 0.5-mA supply current of the LMC7101 extends battery life in portable applications, and may allow the reduction of the size of batteries in some applications.

Feature Description (continued)

7.3.1.7 Wide Voltage Range

The LMC7101 is characterized at 15 V, 5 V and 3 V. Performance data is provided at these popular voltages. This wide voltage range makes the LMC7101 a good choice for devices where the voltage may vary over the life of the batteries.

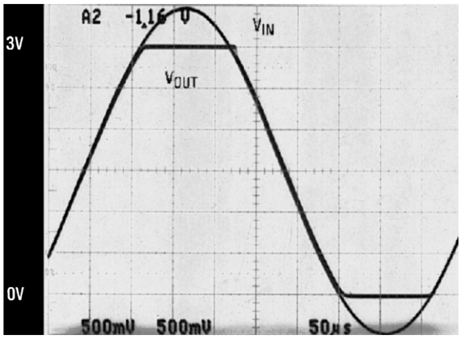
7.4 Device Functional Modes

7.4.1 Input Common Mode

7.4.1.1 Voltage Range

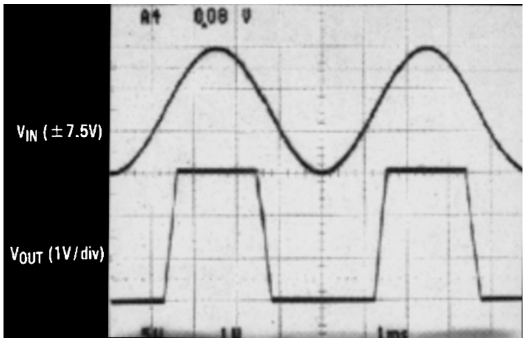
The LMC7101 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. Figure 61 shows an input voltage exceeding both supplies with no resulting phase inversion of the output.

The absolute maximum input voltage is 300-mV beyond either rail at room temperature. Voltages greatly exceeding this maximum rating, as in Figure 62, can cause excessive current to flow in or out of the input pins, thus adversely affecting reliability.



An input voltage signal exceeds the LMC7101 power supply voltages with no output phase inversion.

Figure 61. Input Voltage



A ±7.5-V input signal greatly exceeds the 3-V supply in Figure 63 causing no phase inversion due to R_I.

Figure 62. Input Signal

Applications that exceed this rating must externally limit the maximum input current to ±5 mA with an input resistor as shown in Figure 63.

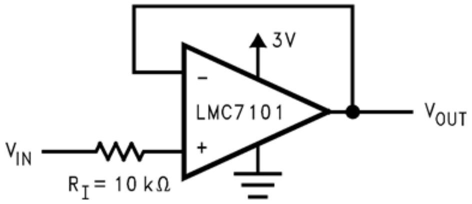


Figure 63. R_I Input Current Protection for Voltages Exceeding the Supply Voltage

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Rail-to-Rail Output

The approximate output resistance of the LMC7101 is 180-Ω sourcing and 130-Ω sinking at V_S = 3 V and 110-Ω sourcing and 80-Ω sinking at V_S = 5 V. Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

8.1.2 Capacitive Load Tolerance

The LMC7101 can typically directly drive a 100-pF load with V_S = 15 V at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of operational amplifiers. The combination of the output impedance and the capacitive load of the operational amplifier induces phase lag, which results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 64. This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.

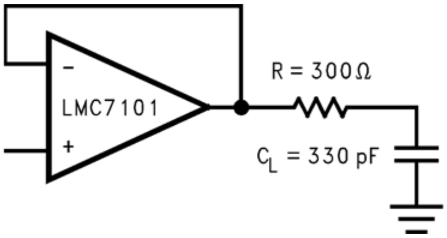


Figure 64. Resistive Isolation of a 330-pF Capacitive Load

8.1.3 Compensating for Input Capacitance When Using Large Value Feedback Resistors

When using very large value feedback resistors, (usually > 500 kΩ) the large feed back resistance can react with the input capacitance due to transducers, photo diodes, and circuit board parasitics to reduce phase margins.

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 65), C_f is first estimated by Equation 1 and Equation 2, which typically provides significant overcompensation.

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \tag{1}$$

$$R_1\ C_{IN} \leq R_2\ C_f \tag{2}$$

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for C_F may be different. The values of C_F must be checked on the actual circuit (refer to *CMOS Quad Operational Amplifier* (SNOSBZ3) for a more detailed discussion).

Application Information (continued)

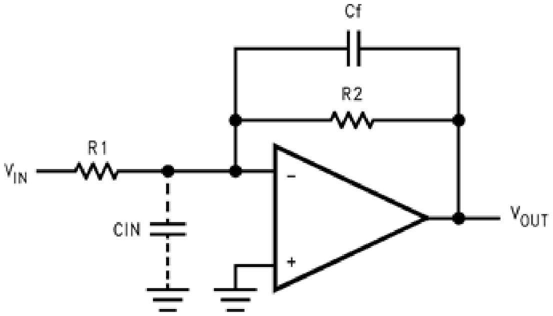


Figure 65. Cancelling the Effect of Input Capacitance

8.2 Typical Application

Figure 66 shows a high input impedance noninverting circuit. This circuit gives a closed-loop gain equal to the ratio of the sum of R1 and R2 to R1 and a closed-loop 3-dB bandwidth equal to the amplifier unity-gain frequency divided by the closed-loop gain. This design has the benefit of a very high input impedance, which is equal to the differential input impedance multiplied by loop gain. (Open loop gain/Closed loop gain.) In DC coupled applications, input impedance is not as important as input current and its voltage drop across the source resistance. The amplifier output will go into saturation if the input is allowed to float, which may be important if the amplifier must be switched from source to source.

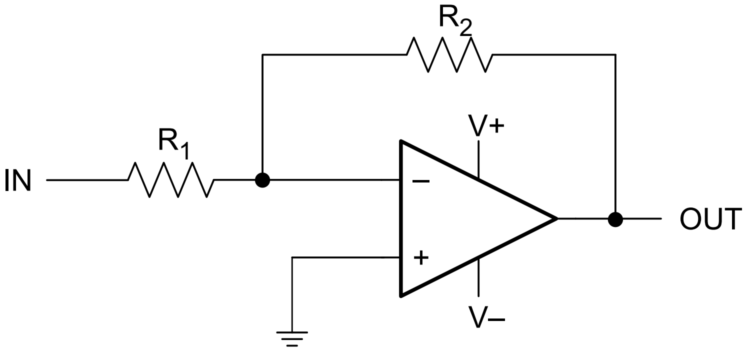


Figure 66. Example Application

Typical Application (continued)

8.2.1 Design Requirements

For this example application, the supply voltage is 5 V, and 100 × ±5% of noninverting gain is necessary. The signal input impedance is approximately 10 kΩ.

8.2.2 Detailed Design Procedure

Use the equation for a noninverting amplifier configuration; G = 1 + R2 / R1, set R1 to 10 kΩ, and R2 to 99 × the value of R1, which would be 990 kΩ. Replacing the 990-kΩ resistor with a more readily available 1-MΩ resistor will result in a gain of 101, which is within the desired gain tolerance. The gain-frequency characteristic of the amplifier and its feedback network must be such that oscillation does not occur. To meet this condition, the phase shift through amplifier and feedback network must never exceed 180° for any frequency where the gain of the amplifier and its feedback network is greater than unity. In practical applications, the phase shift must not approach 180° because this is the situation of conditional stability. The most critical case occurs when the attenuation of the feedback network is zero.

8.2.3 Application Curve

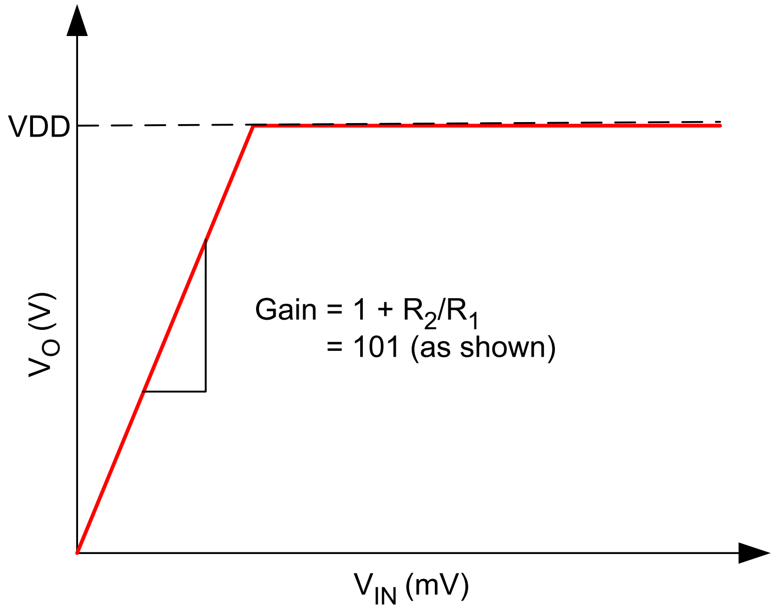


Figure 67. Output Response

9 Power Supply Recommendations

For proper operation, the power supplies must be decoupled. For supply decoupling, TI recommends placing 10-nF to 1-µF capacitors as close as possible to the operational-amplifier power supply pins. For single supply configurations, place a capacitor between the V^+ and V^- supply pins. For dual supply configurations, place one capacitor between V^+ and ground, and place a second capacitor between V^- and ground. Bypass capacitors must have a low ESR of less than 0.1 Ω.

10 Layout

10.1 Layout Guidelines

Care must be taken to minimize the loop area formed by the bypass capacitor connection between supply pins and ground. A ground plane underneath the device is recommended; any bypass components to ground must have a nearby via to the ground plane. The optimum bypass capacitor placement is closest to the corresponding supply pin. Use of thicker traces from the bypass capacitors to the corresponding supply pins will lower the power-supply inductance and provide a more stable power supply.

The feedback components must be placed as close as possible to the device to minimize stray parasitics.

10.2 Layout Example

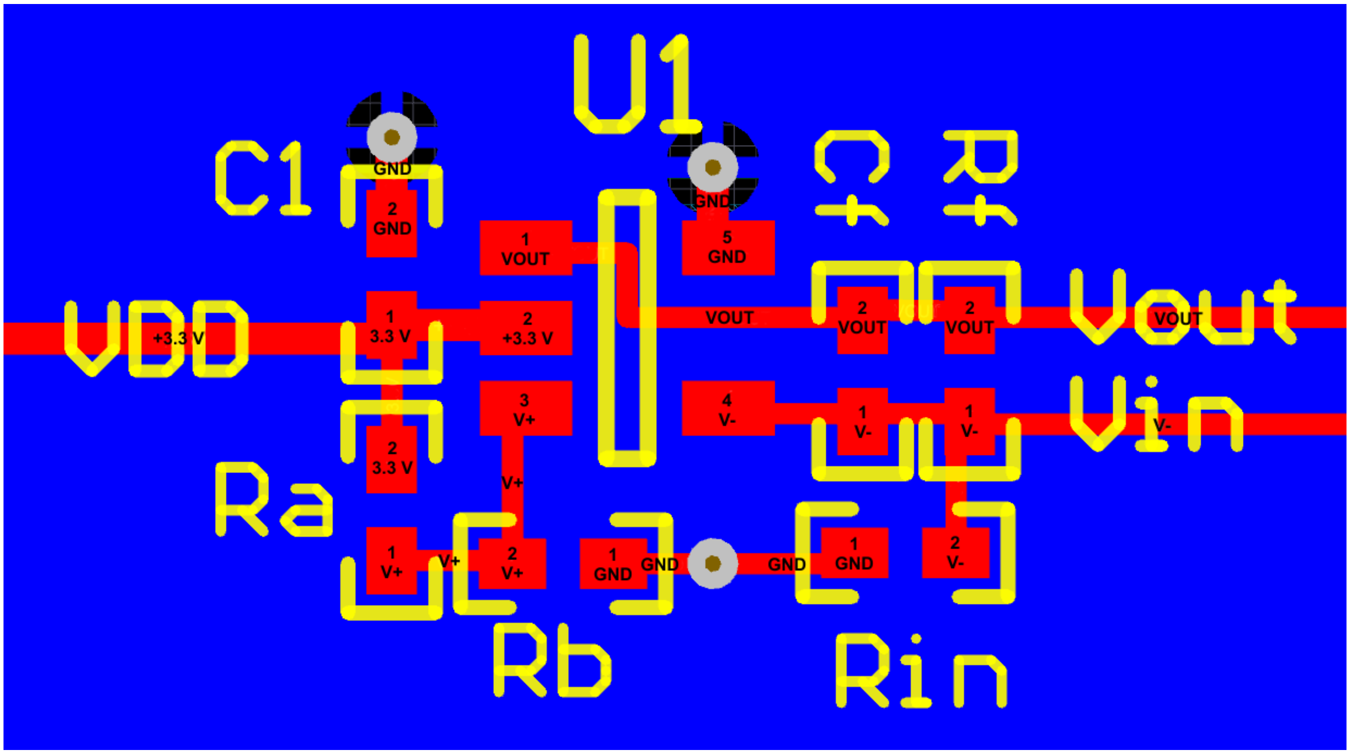


Figure 68. LMC7101 Example Layout

11 Device and Documentation Support

11.1 Documentation Support

For additional information, see *LMC660 CMOS Quad Operational Amplifier* (SNOSBZ3).

11.2 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMC7101	Click here	Click here	Click here	Click here	Click here
LMC7101Q-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC7101AIM5	LIFEBUY	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	A00A	
LMC7101AIM5/NOPB	LIFEBUY	SOT-23	DBV	5	1000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	A00A	
LMC7101AIM5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	A00A	Samples
LMC7101BIM5	LIFEBUY	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	A00B	
LMC7101BIM5/NOPB	LIFEBUY	SOT-23	DBV	5	1000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	A00B	
LMC7101BIM5X	LIFEBUY	SOT-23	DBV	5	3000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	A00B	
LMC7101BIM5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	A00B	Samples
LMC7101QM5/NOPB	LIFEBUY	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AT6A	
LMC7101QM5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	AT6A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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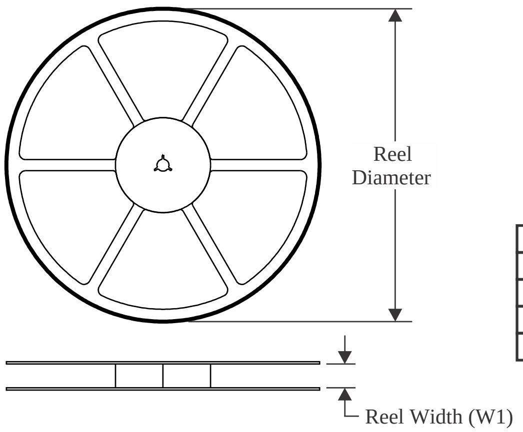
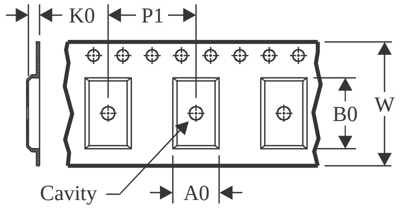
TAPE AND REEL INFORMATION

REEL DIMENSIONS

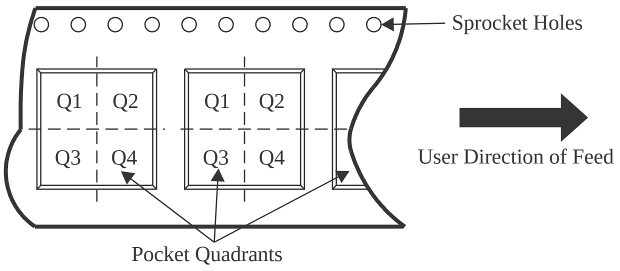


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

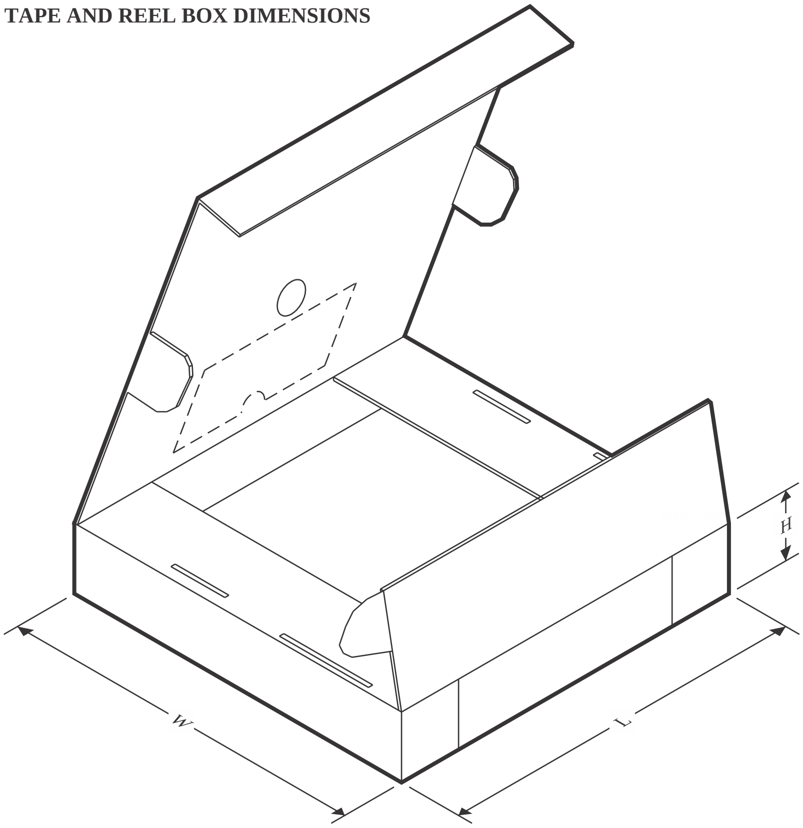
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC7101AIM5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101AIM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101AIM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101BIM5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101BIM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101BIM5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101BIM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101BIM5X/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101QM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101QM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

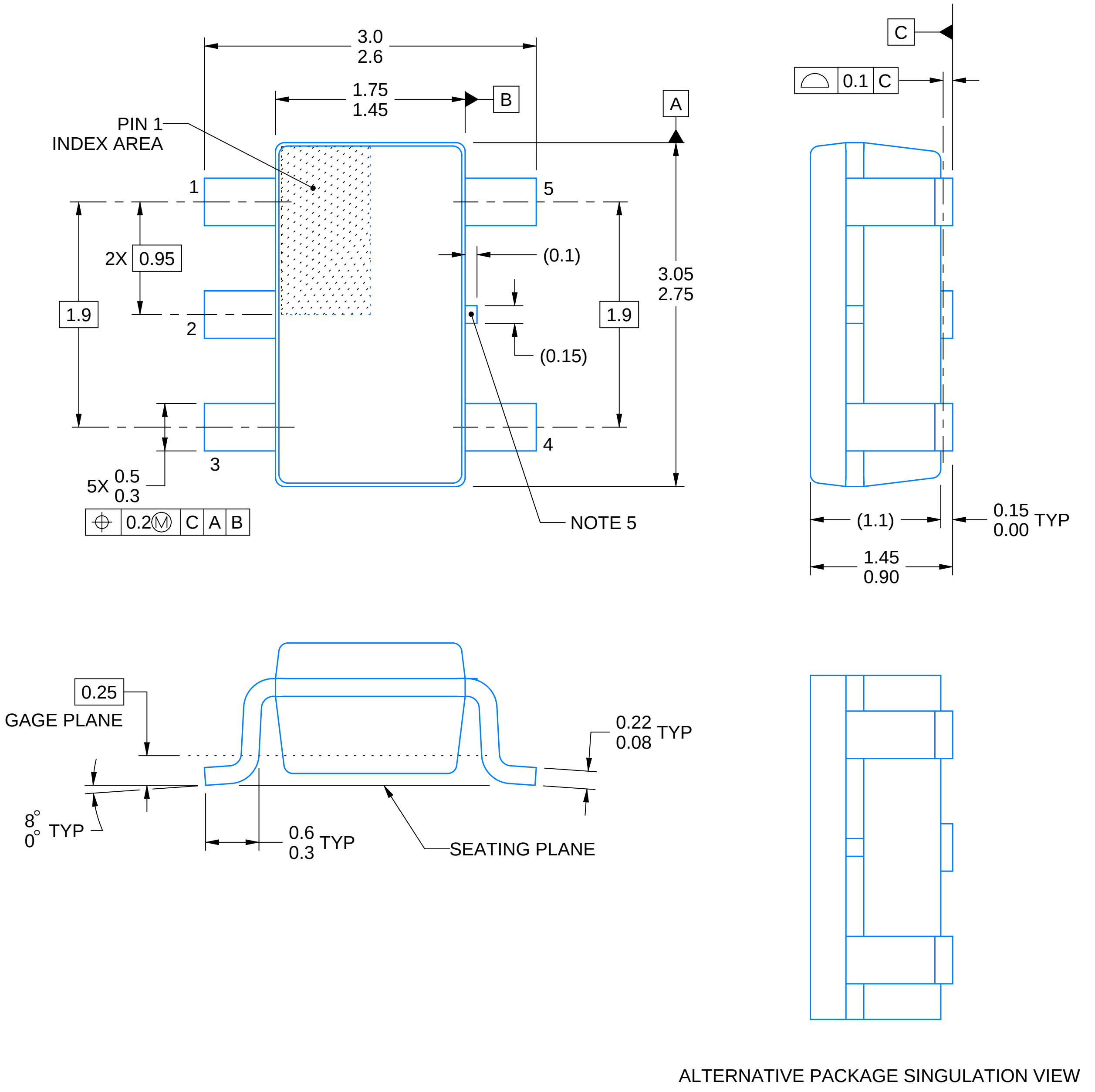
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC7101AIM5	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMC7101AIM5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMC7101AIM5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMC7101BIM5	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMC7101BIM5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMC7101BIM5X	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMC7101BIM5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMC7101BIM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMC7101QM5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMC7101QM5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

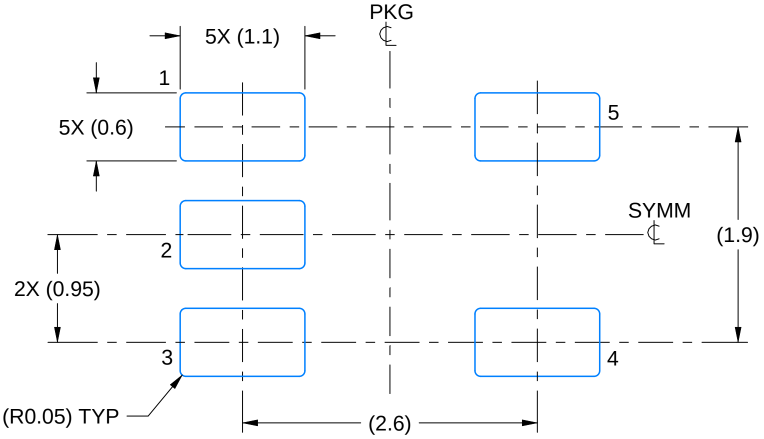


ALTERNATIVE PACKAGE SINGULATION VIEW

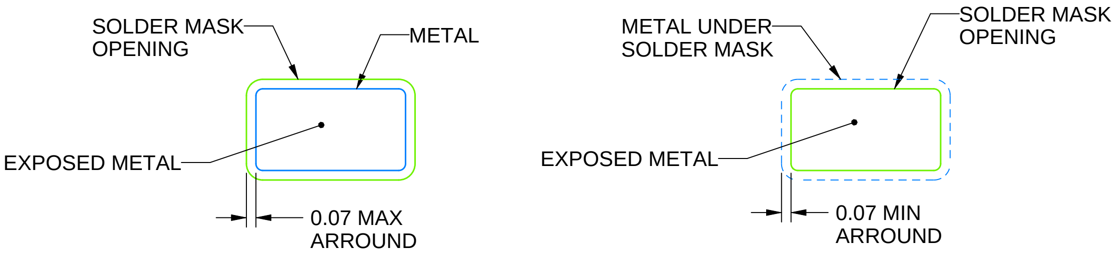
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



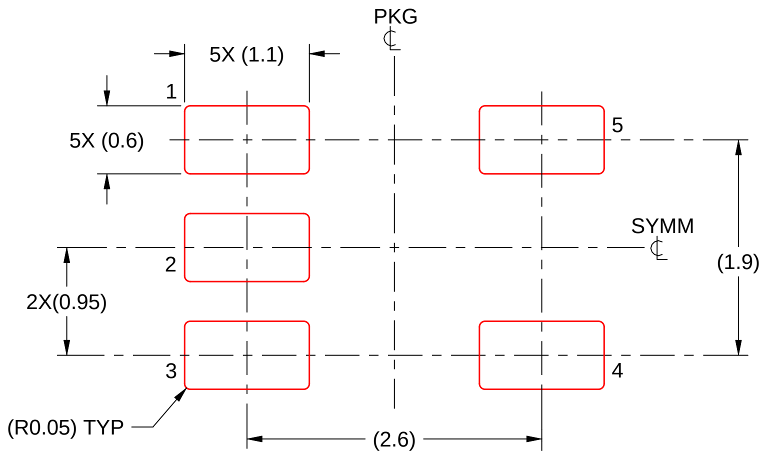
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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