



**THE DATASHEET OF  
IRS2186STRPBF**



## High and Low Side Driver

### Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage
- dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V and 5 V logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5 V offset
- Lower di/dt gate driver for better noise immunity
- Output source/sink current 4 A / 4 A
- RoHS compliant

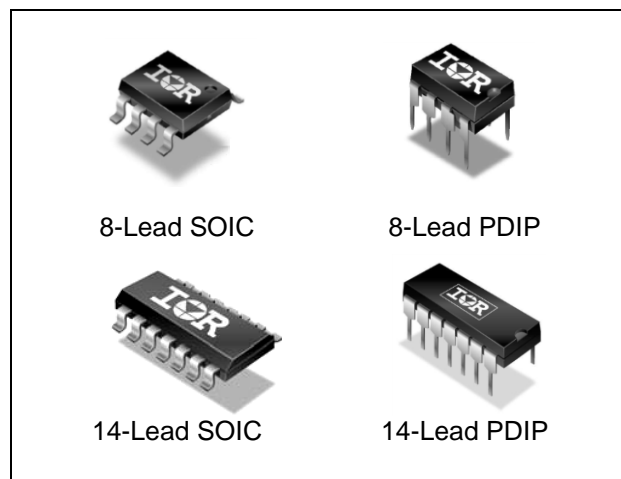
### Description

The IRS2186(4) are high voltage, high speed power MOSFET and IGBT drivers with independent high-side and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

### Product Summary

$V_{\text{OFFSET}}$	600 V
$I_{\text{O+/-}}$	4 A / 4 A
$V_{\text{OUT}}$	10 V – 20 V
Ton/off (typ.)	170 & 170 ns

### Package Options

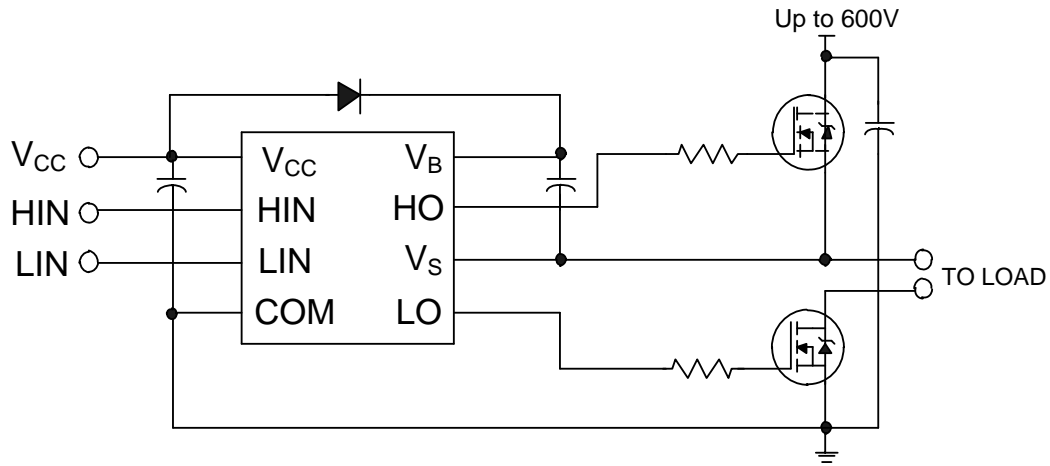


### Ordering Information

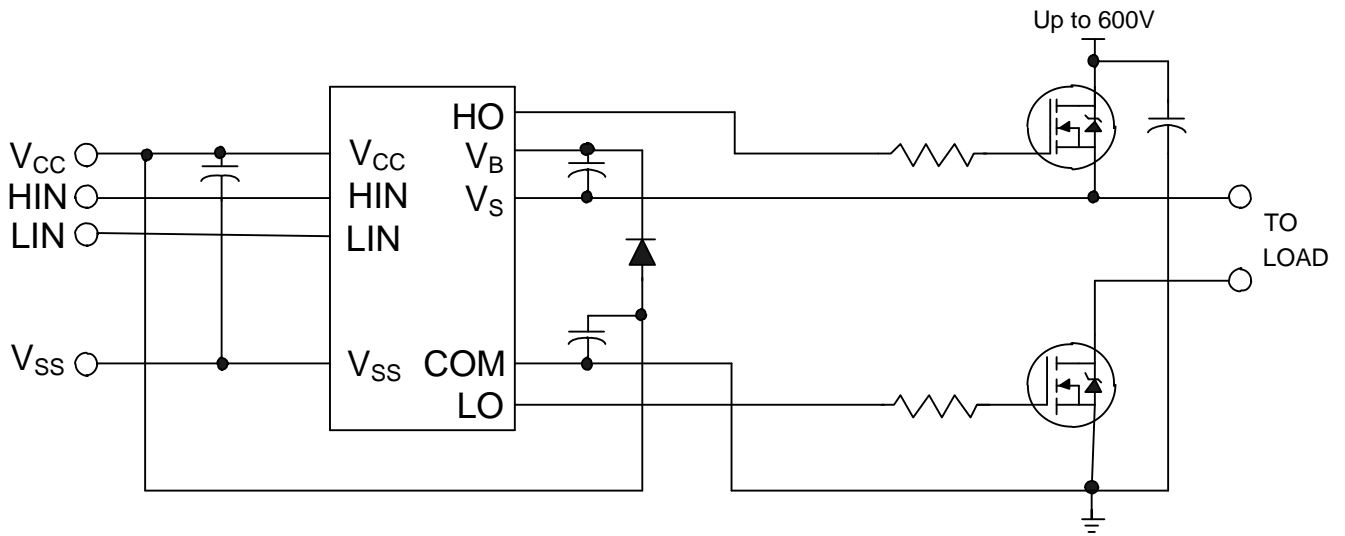
Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRS2186SPBF	SO8N	Tube	95	IRS2186SPBF
IRS2186SPBF	SO8N	Tape and Reel	2500	IRS2186STRPBF
IRS21864SPBF	SO14N	Tube	55	IRS21864SPBF
IRS21864SPBF	SO14N	Tape and Reel	2500	IRS21864STRPBF
IRS2186PBF	PDIP8	Tube	50	IRS2186PBF
IRS21864PBF	PDIP14	Tube	25	IRS21864PBF

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**Typical Connection Diagram**



IRS2186(S)



IRS21864(S)

(Refer to Lead Assignments for correct pin configuration). These diagrams show electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
$V_B$	High side floating absolute voltage	-0.3	620 <sup>†</sup>	V	
$V_S$	High side floating supply offset voltage	$V_B - 20$	$V_B + 0.3$		
$V_{HO}$	High side floating output voltage	$V_S - 0.3$	$V_B + 0.3$		
$V_{CC}$	Low side and logic fixed supply voltage	-0.3	20 <sup>†</sup>		
$V_{LO}$	Low side output voltage	-0.3	$V_{CC} + 0.3$		
$V_{IN}$	Logic input voltage (HIN & LIN)	$V_{SS} - 0.3$	$V_{CC} + 0.3$		
$V_{SS}$	Logic ground (IRS21864)	$V_{CC} - 20$	$V_{CC} + 0.3$		
$dV_S/dt$	Allowable offset supply voltage transient	—	50		V/ns
$P_D$	Package power dissipation @ $T_A \leq +25^\circ\text{C}$	8 lead PDIP	—	1	W
		8 lead SOIC	—	0.625	
		14 lead PDIP	—	1.6	
		14 lead SOIC	—	1	
$R_{thJA}$	Thermal resistance, junction to ambient	8 lead PDIP	—	125	°C/W
		8 lead SOIC	—	200	
		14 lead PDIP	—	75	
		14 lead SOIC	—	120	
$T_J$	Junction temperature	—	150	°C	
$T_S$	Storage temperature	-50	150		
$T_L$	Lead temperature (soldering, 10 seconds)	—	300		

## Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The  $V_S$  and  $V_{SS}$  offset rating is tested with all supplies biased at 15 V differential.

Symbol	Definition	Min.	Max.	Units
$V_B$	High side floating absolute voltage	$V_S + 10$	$V_S + 20$	V
$V_S$	High side floating supply offset voltage	††	600	
$V_{HO}$	High side floating output voltage	$V_S$	$V_B$	
$V_{CC}$	Low side and logic fixed supply voltage	10	20	
$V_{LO}$	Low side output voltage	0	$V_{CC}$	
$V_{IN}$	Logic input voltage (HIN & LIN)	$V_{SS}$	$V_{CC}$	
$V_{SS}$	Logic ground (IRS21864)	-5	5	
$T_A$	Ambient temperature	-40	125	°C

† All supplies are fully tested at 25 V and an internal 20 V clamp exists for each supply

†† Logic operational for  $V_S$  of -5 V to 600 V. Logic state held for  $V_S$  of -5 V to  $-V_{BS}$  (Please refer to the Design Tip DT97-3 for more details)

### Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15 V,  $V_{SS}$  = COM,  $C_L$  = 1000 pF and  $T_A$  = 25 °C unless otherwise specified.

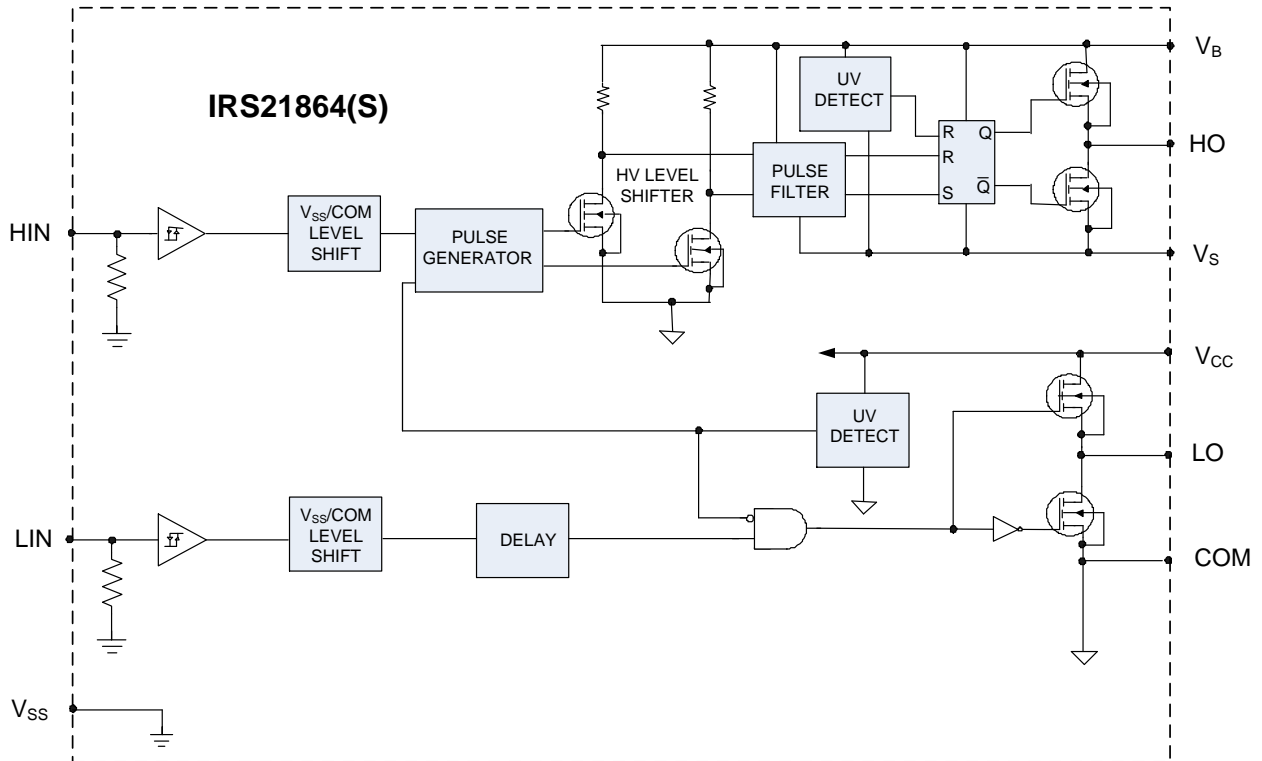
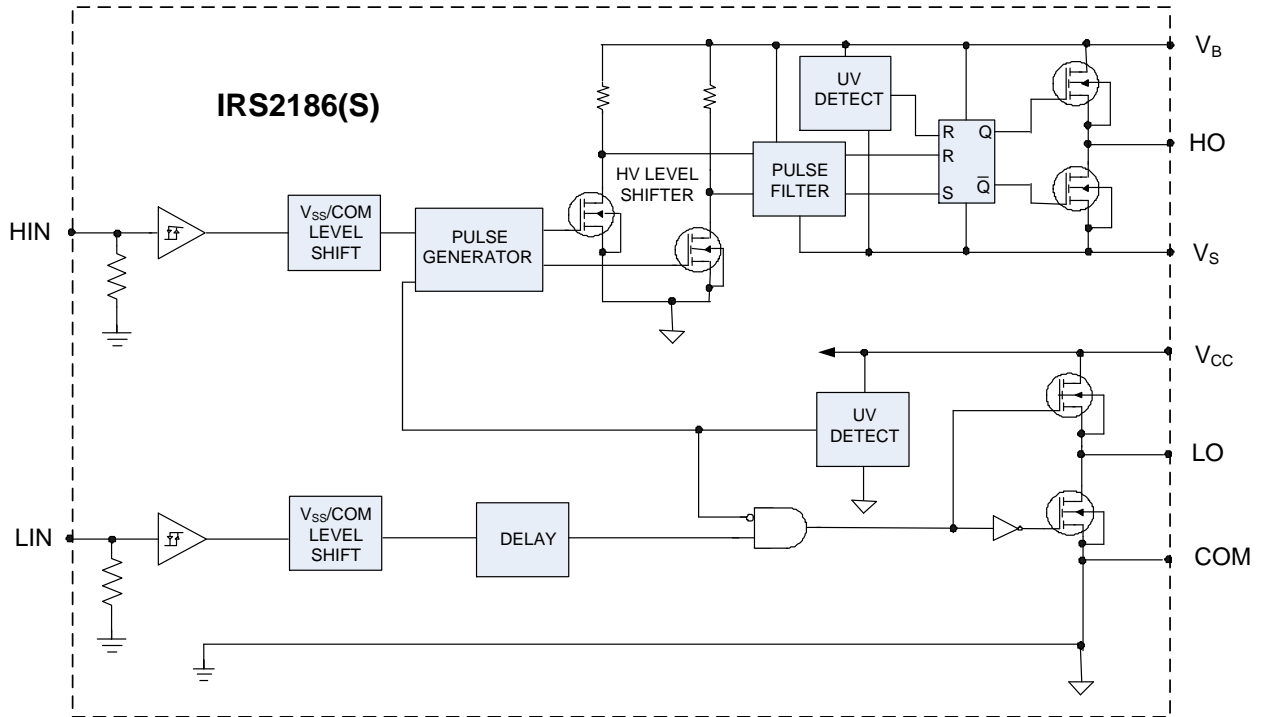
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	—	170	250	ns	$V_S = 0$ V
$t_{off}$	Turn-off propagation delay	—	170	250		$V_S = 0$ V or 600 V
$t_r$	Turn-on rise time	—	22	38		$V_S = 0$ V
$t_f$	Turn-off fall time	—	18	30		
MT	Delay matching, HS & LS turn on/off	—	0	35		

### Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15 V,  $V_{SS}$  = COM, and  $T_A$  = 25 °C unless otherwise specified. The  $V_{IL}$ ,  $V_{IH}$ , and  $I_{IN}$  parameters are referenced to  $V_{SS}/COM$  and are applicable to the respective input leads  $H_{IN}$  and  $L_{IN}$ . The  $V_O$ ,  $I_O$ , and  $R_{ON}$  parameters are referenced to COM and are applicable to the respective output leads:  $H_O$  and  $L_O$ .

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{IH}$	Logic "1" input voltage	2.5	—	—	V	$V_{CC} = 10$ V to 20 V $I_O = 0$ A
$V_{IL}$	Logic "0" input voltage	—	—	0.8		
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	—	—	1.4		
$V_{OL}$	Low level output voltage, $V_O$	—	—	0.15		
$I_{LK}$	Offset supply leakage current	—	—	50	$\mu$ A	$V_B = V_S = 600$ V $V_{IN} = 0$ V or 5 V
$I_{QBS}$	Quiescent $V_{BS}$ supply current	20	60	150		
$I_{QCC}$	Quiescent $V_{CC}$ supply current	50	120	240		
$I_{IN+}$	Logic "1" input bias current	—	25	60		
$I_{IN-}$	Logic "0" input bias current	—	—	5		$V_{IN} = 0$ V
$V_{CCUV+}$ $V_{BSUV+}$	$V_{CC}$ and $V_{BS}$ supply undervoltage positive going threshold	8	8.9	9.8	V	
$V_{CCUV-}$ $V_{BSUV-}$	$V_{CC}$ and $V_{BS}$ supply undervoltage negative going threshold	7.4	8.2	9		
$V_{CCUVH}$ $V_{BSUVH}$	Hysteresis	0.3	0.7	—		
$I_{O+}$	Output high short circuit pulsed current	2	4	—	A	$V_O = 0$ V, $PW \leq 10$ $\mu$ s
$I_{O-}$	Output low short circuit pulsed current	2	4	—		$V_O = 15$ V, $PW \leq 10$ $\mu$ s

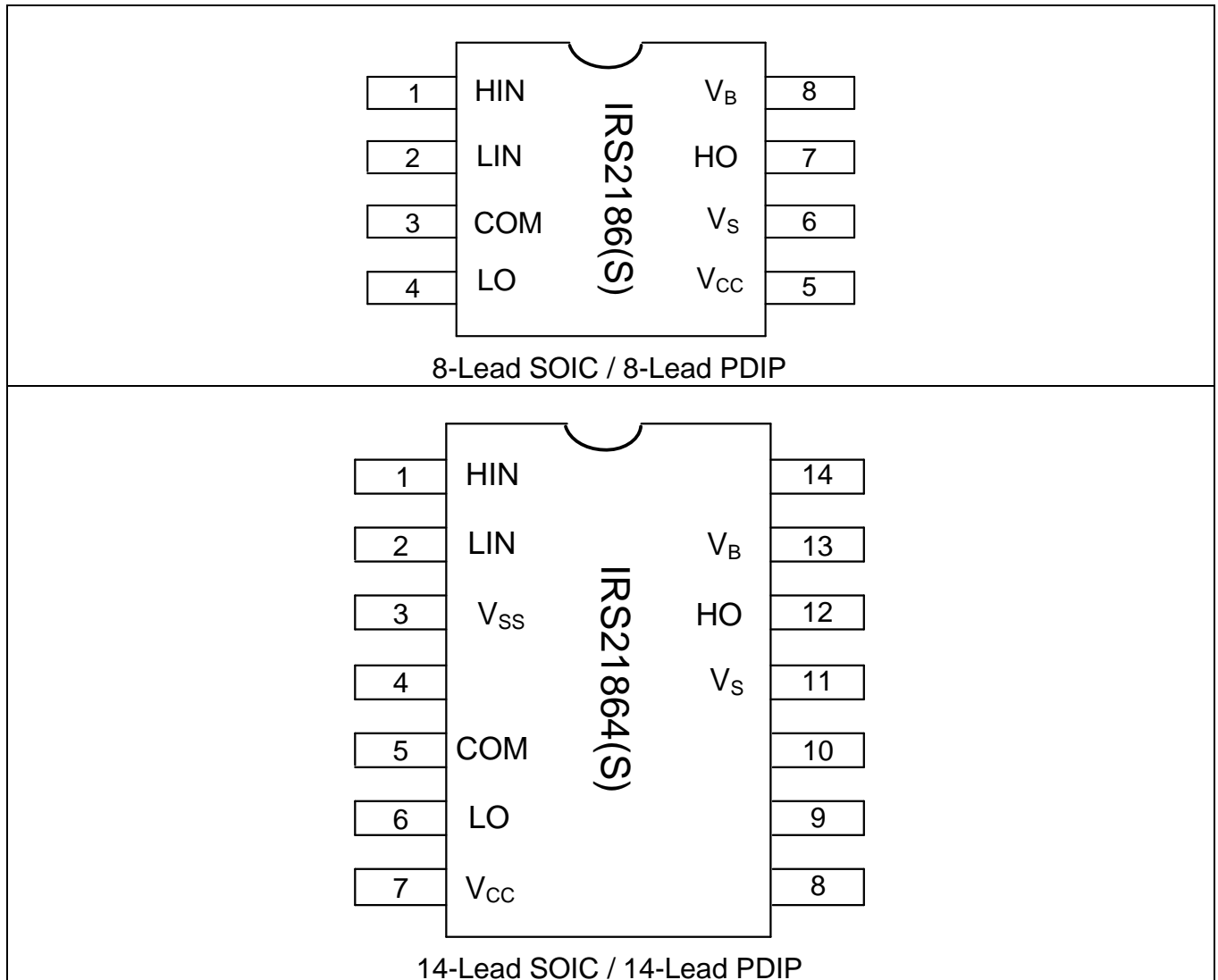
**Functional Block Diagram**



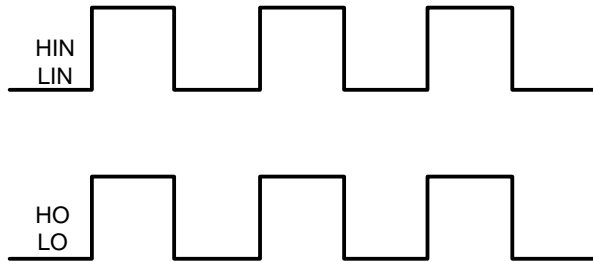
### Lead Definitions

Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase
LIN	Logic input for low side gate driver output (LO), in phase
V <sub>SS</sub>	Logic ground (IRS21864)
V <sub>B</sub>	High side floating supply
HO	High side gate drive output
V <sub>S</sub>	High side floating supply return
V <sub>CC</sub>	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

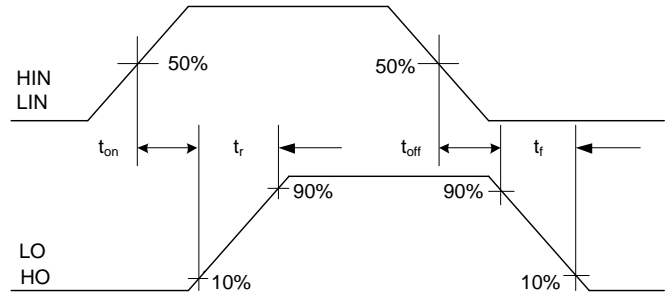
### Lead Assignments



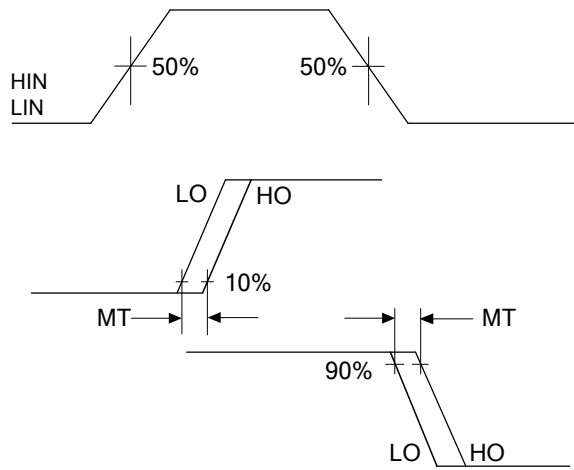
**Application Information and Additional Details**



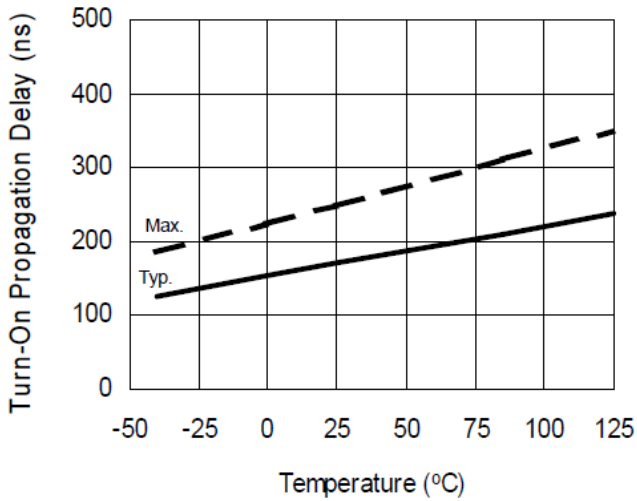
**Figure 1. Input/Output Timing Diagram**



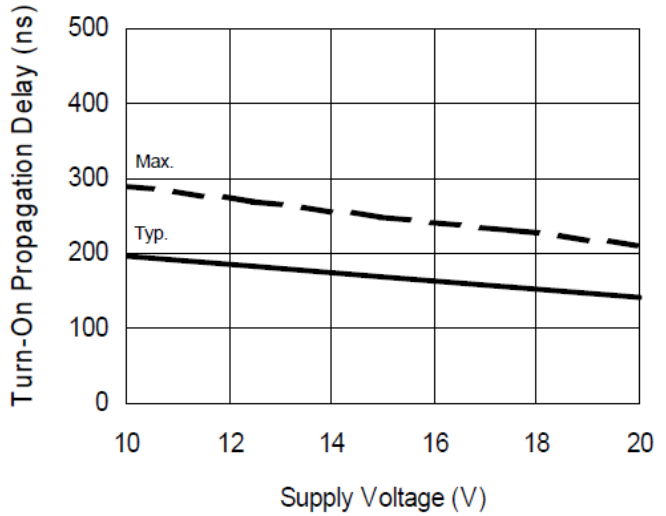
**Figure 2. Switching Time Waveform Definitions**



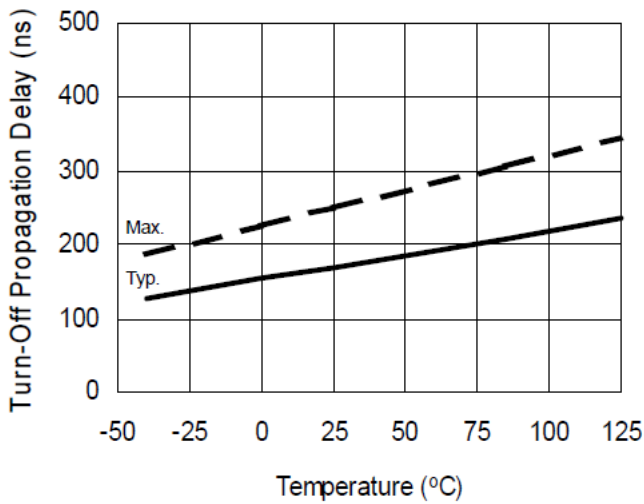
**Figure 3. Delay Matching Waveform Definitions**



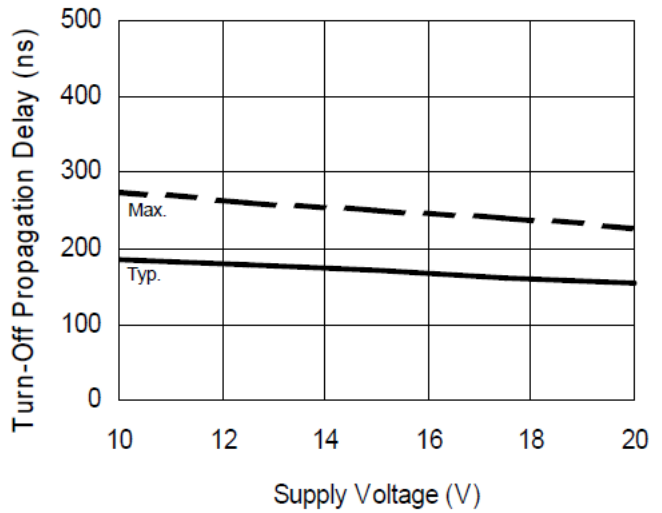
**Figure 4A. Turn-On Propagation Delay vs. Temperature**



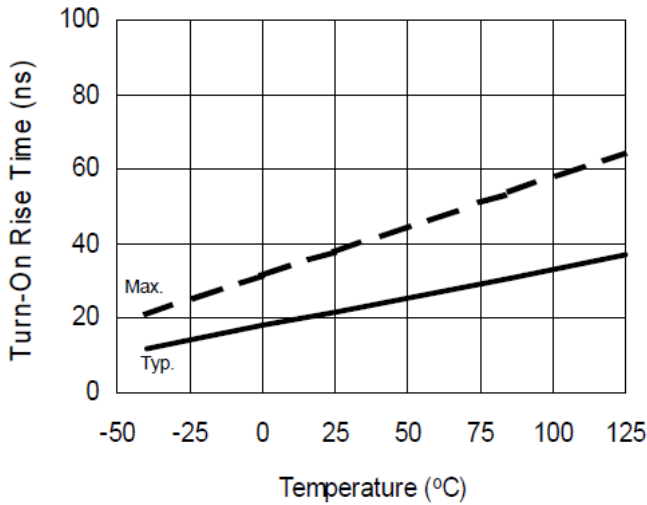
**Figure 4B. Turn-on Propagation Delay vs. Supply Voltage**



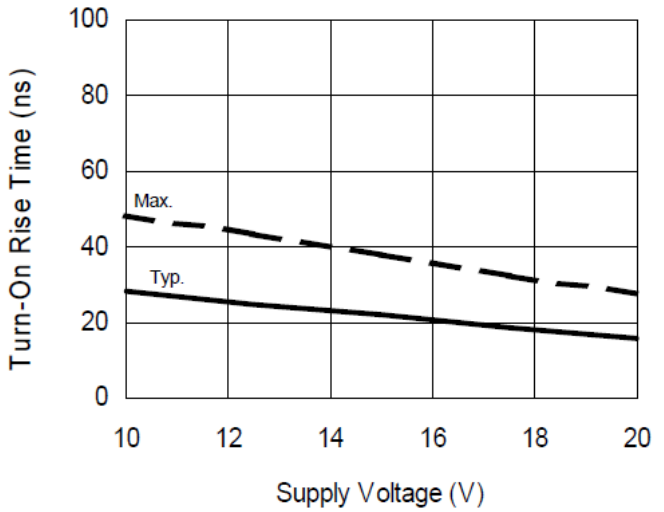
**Figure 5A. Turn-Off Propagation Delay vs. Temperature**



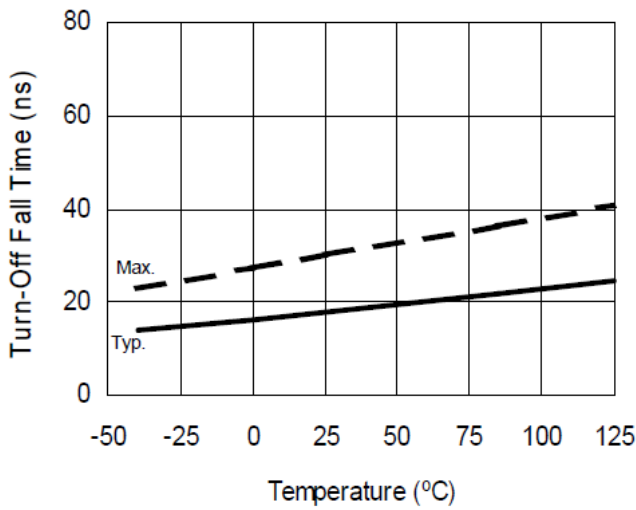
**Figure 5B. Turn-Off Propagation Delay vs. Supply Voltage**



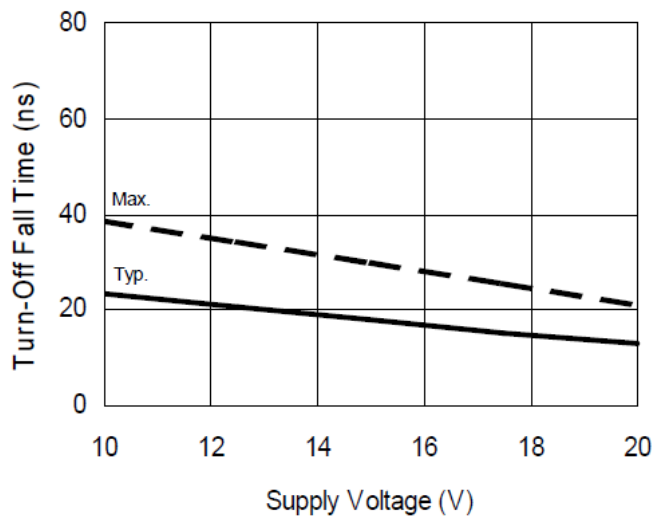
**6A. Turn-On Rise Time vs. Temperature**



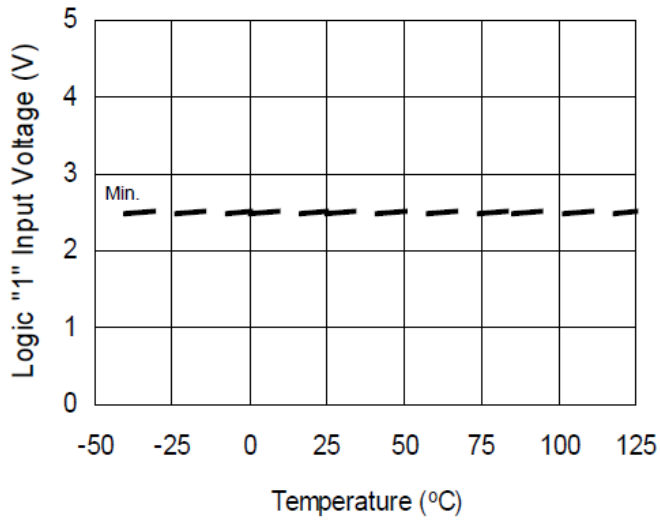
**Figure 6B. Turn-On Rise Time vs. Supply Voltage**



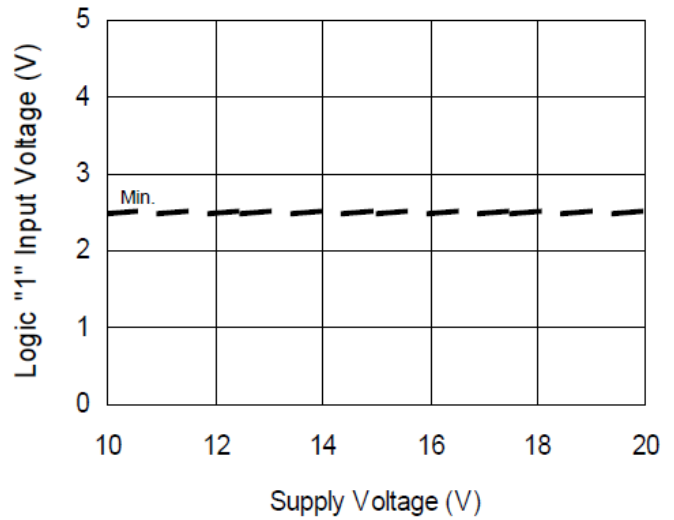
**Figure 7A. Turn-Off Fall Time vs. Temperature**



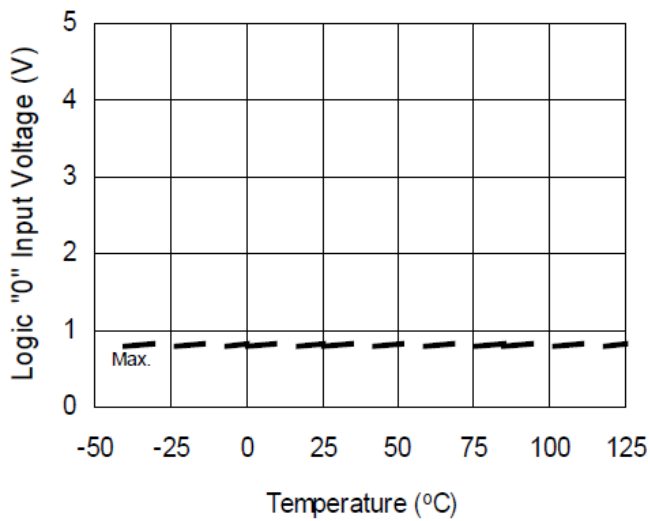
**Figure 7B. Turn-Off Fall Time vs. Supply Voltage**



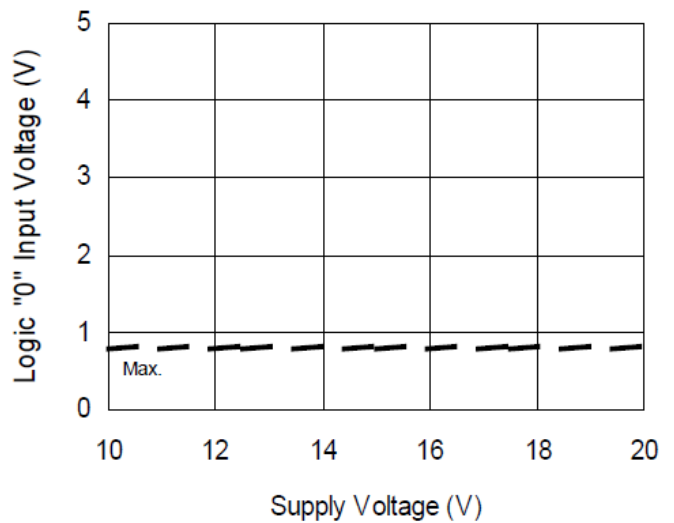
**Figure 8A. Logic "1" Input Voltage vs. Temperature**



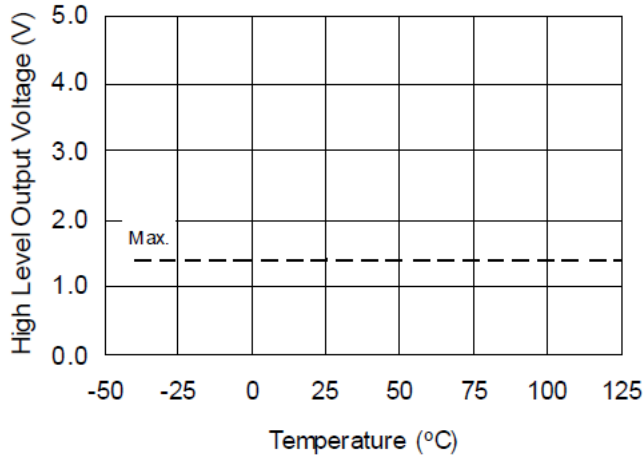
**Figure 8B. Logic "1" Input Voltage vs. Supply Voltage**



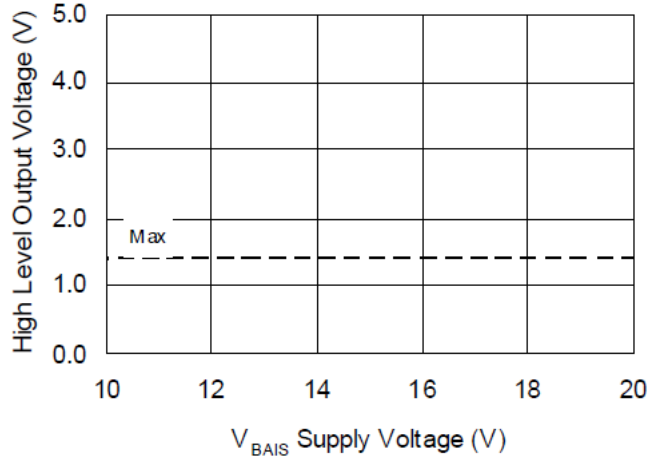
**Figure 9A. Logic "0" Input Voltage vs. Temperature**



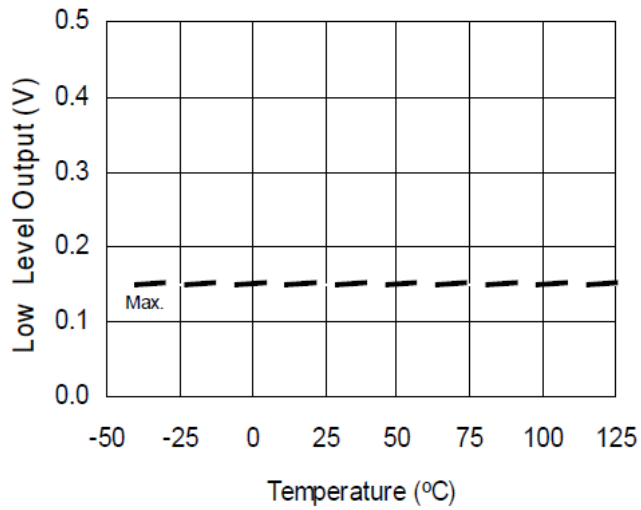
**Figure 9B. Logic "0" Input Voltage vs. Supply Voltage**



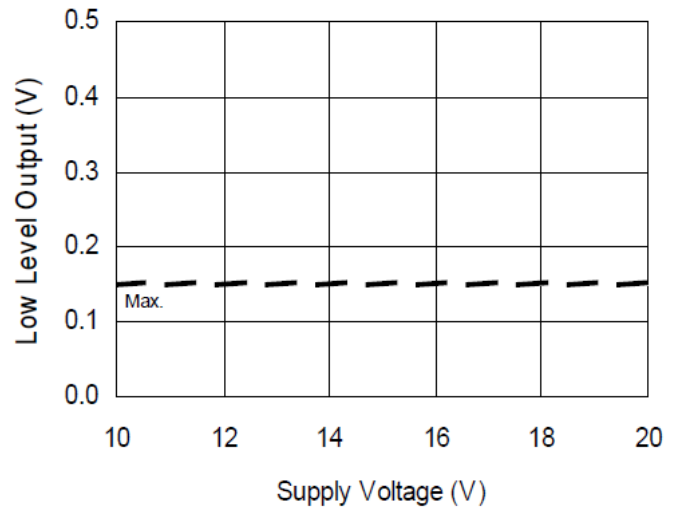
**Figure 10A. High Level Output Voltage vs. Temperature (Io = 0mA)**



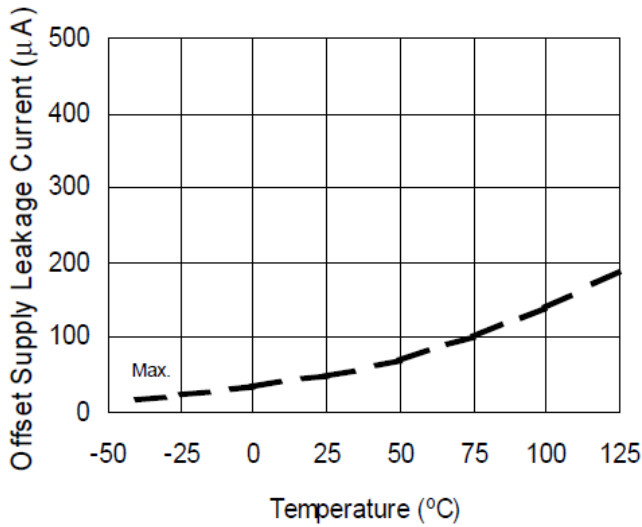
**Figure 10B. High Level Output Voltage vs. Supply Voltage (Io = 0mA)**



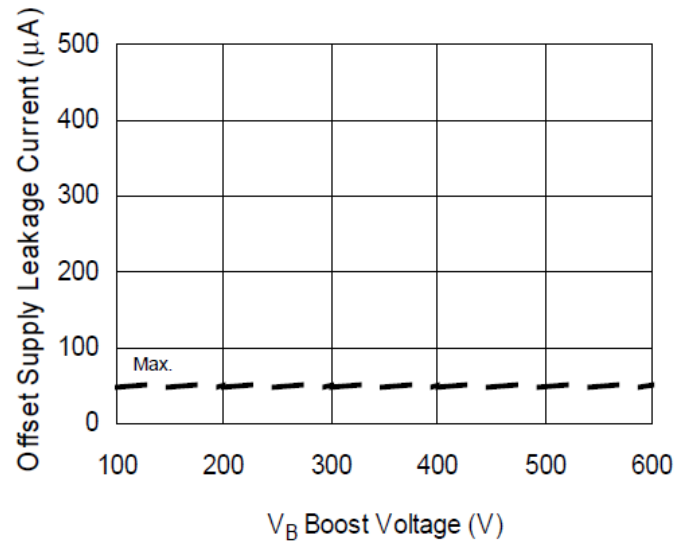
**Figure 11A. Low Level Output vs. Temperature**



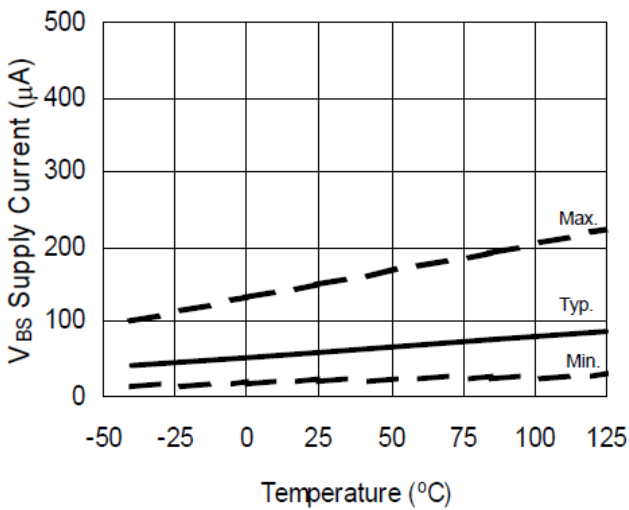
**Figure 11B. Low Level Output vs. Supply Voltage**



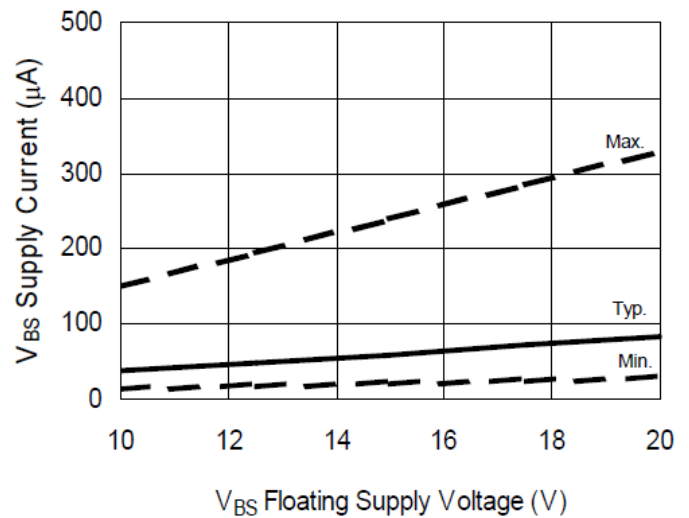
**Figure 12A. Offset Supply Leakage Current**



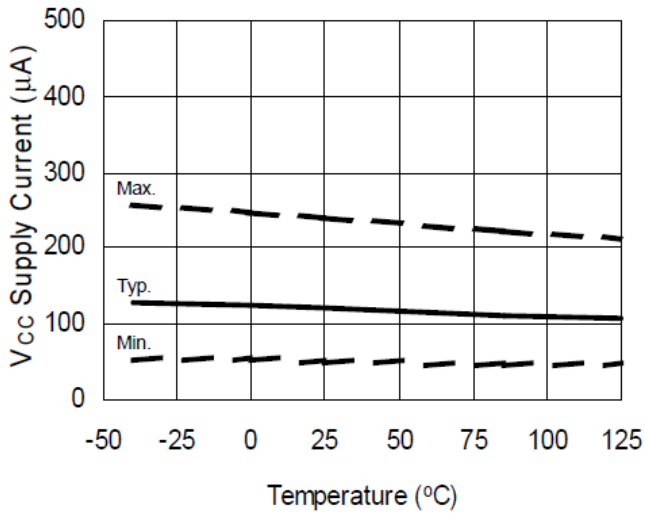
**Figure 12B. Offset Supply Leakage Current vs. V<sub>B</sub> Boost Voltage**



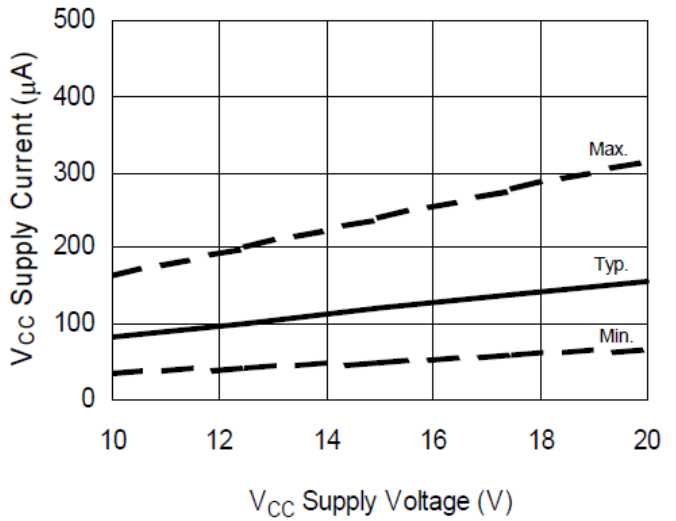
**Figure 13A. V<sub>BS</sub> Supply Current vs. Temperature**



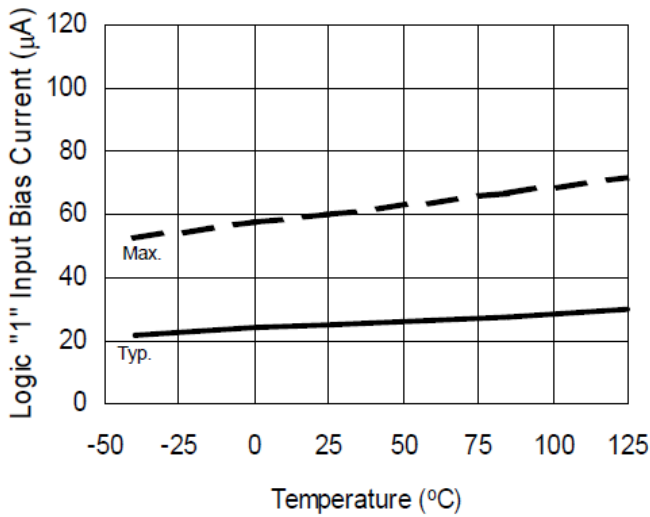
**Figure 13B. V<sub>BS</sub> Supply Current vs. V<sub>BS</sub> Floating Supply Voltage**



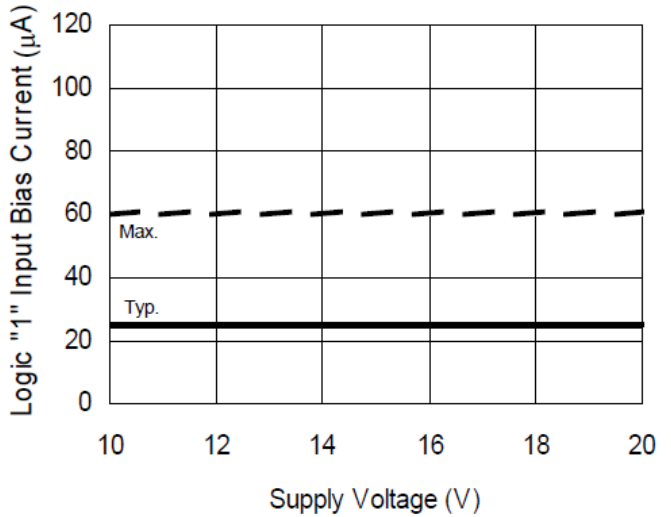
**Figure 14A.  $V_{CC}$  Supply Current vs. Temperature**



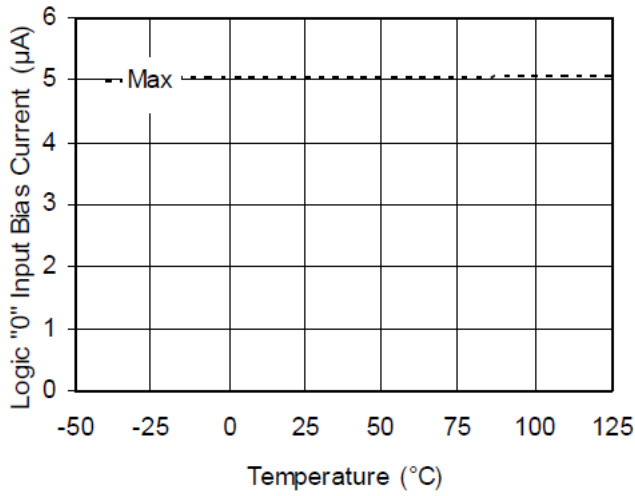
**Figure 14B.  $V_{CC}$  Supply Current vs. Supply Voltage**



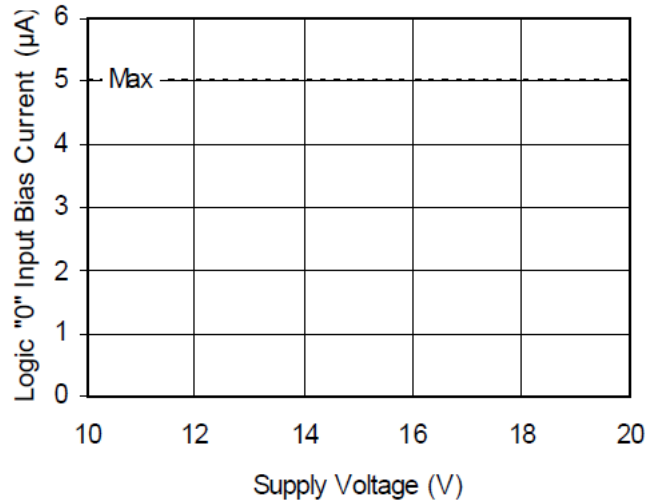
**Figure 15A. Logic "1" Input Bias Current vs. Temperature**



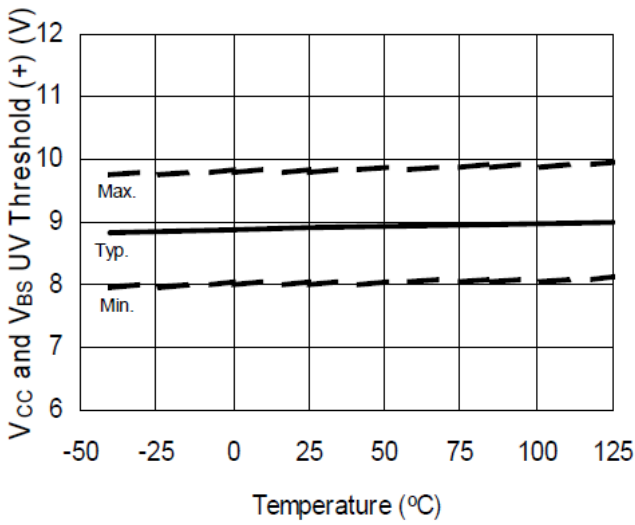
**Figure 15B. Logic "1" Input Bias Current vs. Supply Voltage**



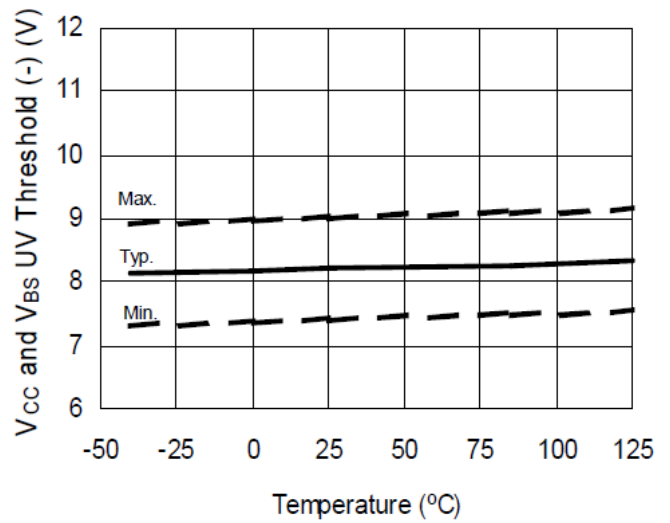
**Figure 16A. Logic "0" Input Bias Current vs. Temperature**



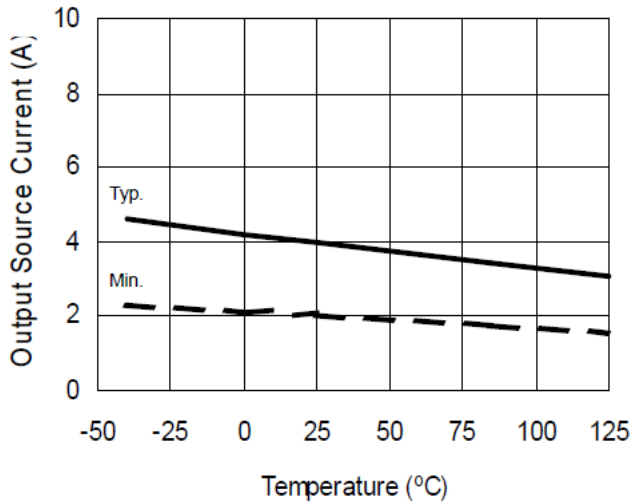
**Figure 16B. Logic "0" Input Bias Current vs. Voltage**



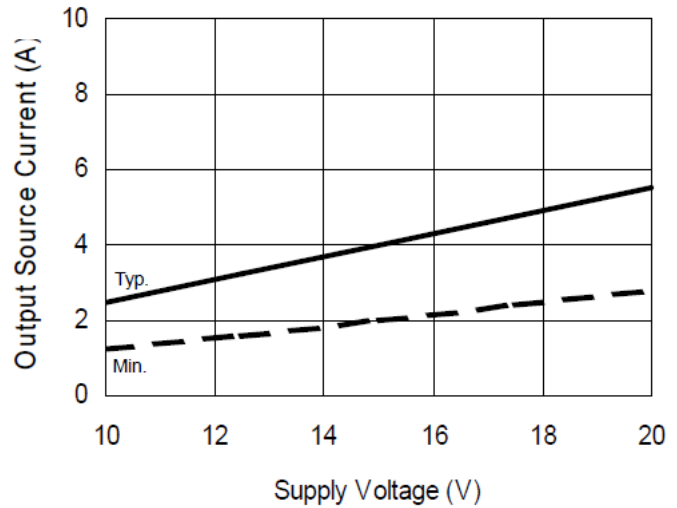
**Figure 17. V<sub>CC</sub> and V<sub>BS</sub> Undervoltage Threshold (+) vs. Temperature**



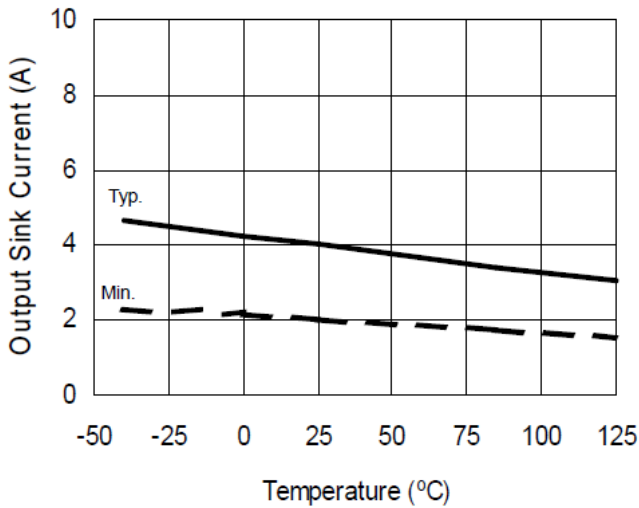
**Figure 18. V<sub>CC</sub> and V<sub>BS</sub> Undervoltage Threshold (-) vs. Temperature**



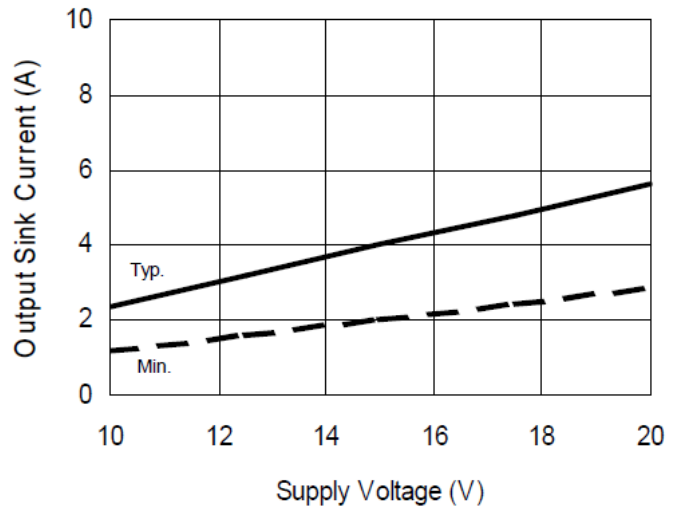
**Figure 19A. Output Source Current vs. Temperature**



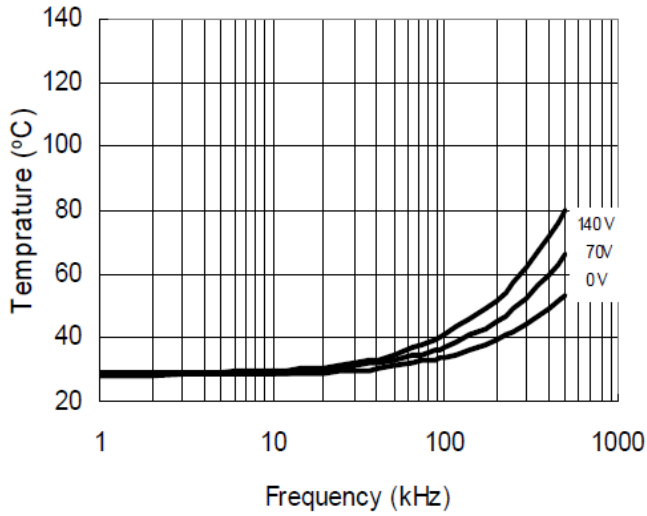
**Figure 19B. Output Source Current vs. Supply Voltage**



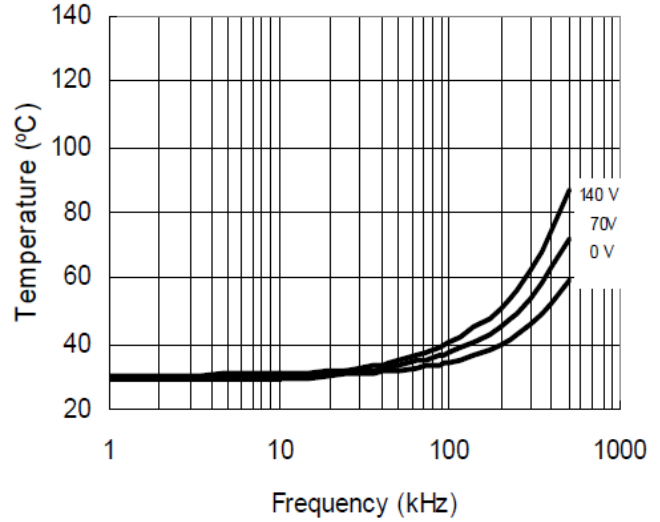
**Figure 20A. Output Sink Current vs. Temperature**



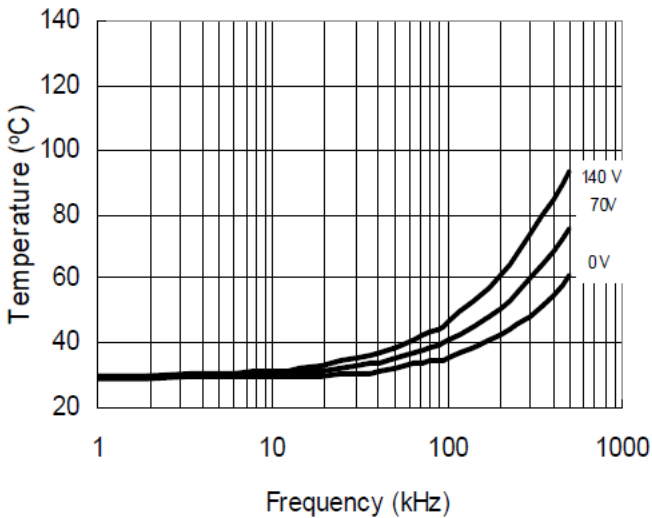
**Figure 10B. Output Sink Current vs. Supply Voltage**



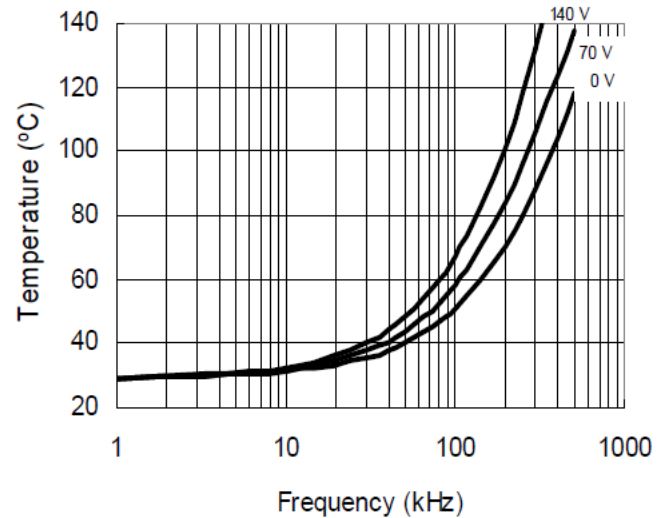
**Figure 21. IRS2186 vs. Frequency (IRFBC20)**  
 $R_{gate} = 33\Omega, V_{CC} = 15V$



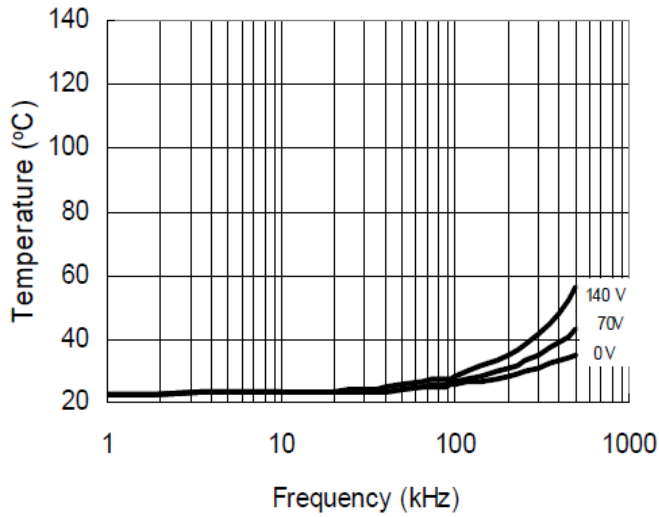
**Figure 22. IRS2186 vs. Frequency (IRFBC30)**  
 $R_{gate} = 22\Omega, V_{CC} = 15V$



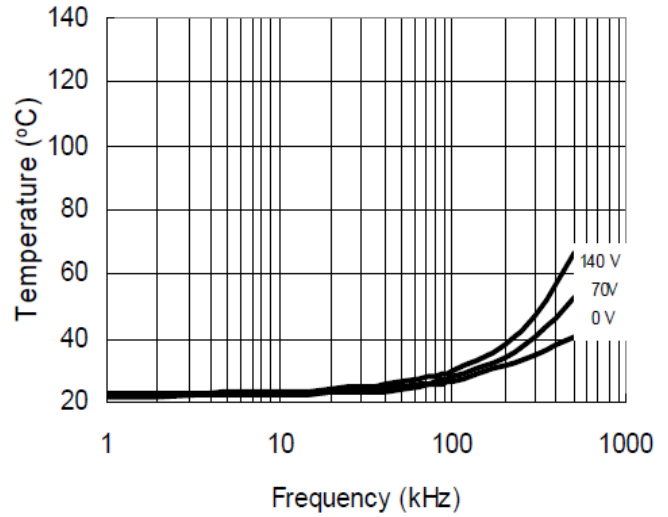
**Figure 23. IRS2186 vs. Frequency (IRFBC40)**  
 $R_{gate} = 15\Omega, V_{CC} = 15V$



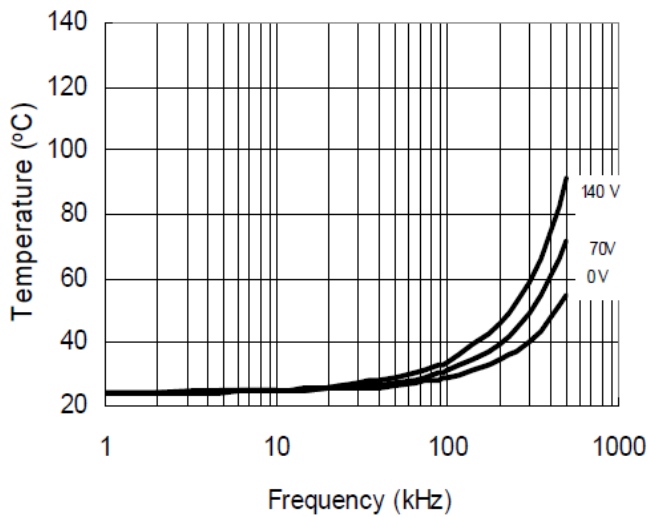
**Figure 24. IRS2186 vs. Frequency (IRFPE50)**  
 $R_{gate} = 10\Omega, V_{CC} = 15V$



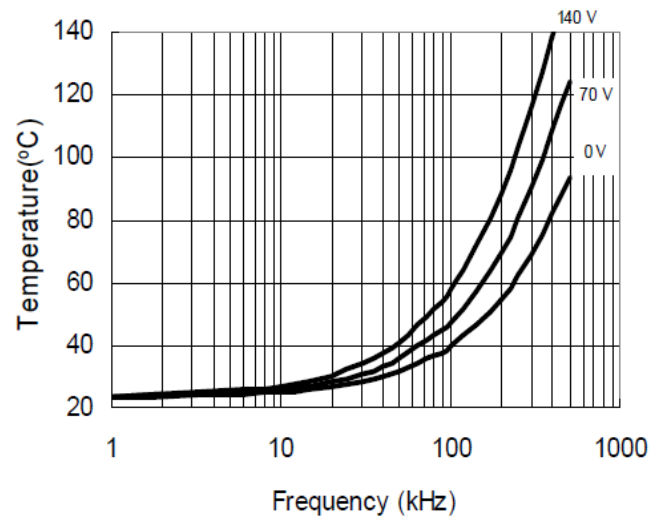
**Figure 25. IRS21864 vs. Frequency (IRFBC20)**  
 $R_{gate} = 33\Omega$ ,  $V_{CC} = 15V$



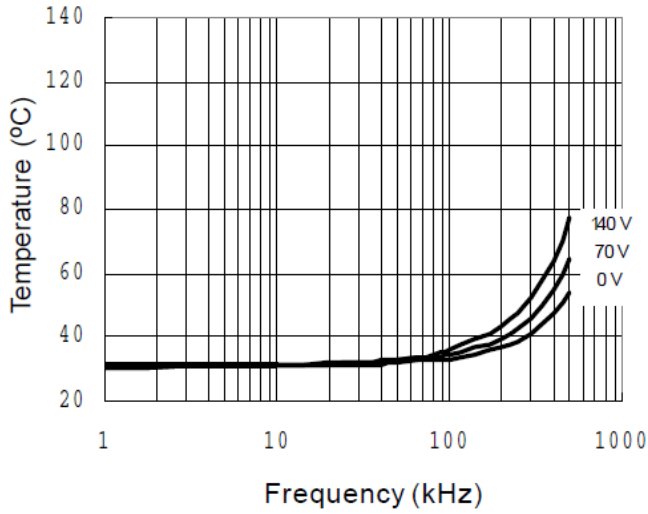
**Figure 26. IRS21864 vs. Frequency (IRFBC30)**  
 $R_{gate} = 22\Omega$ ,  $V_{CC} = 15V$



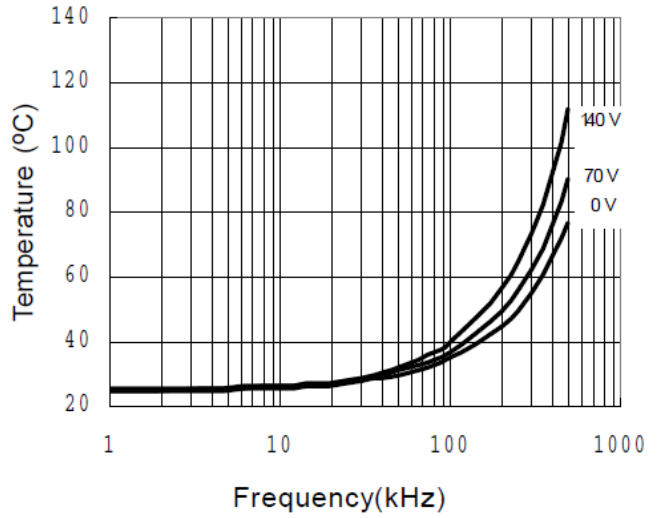
**Figure 27. IRS21864 vs. Frequency (IRFBC40)**  
 $R_{gate} = 15\Omega$ ,  $V_{CC} = 15V$



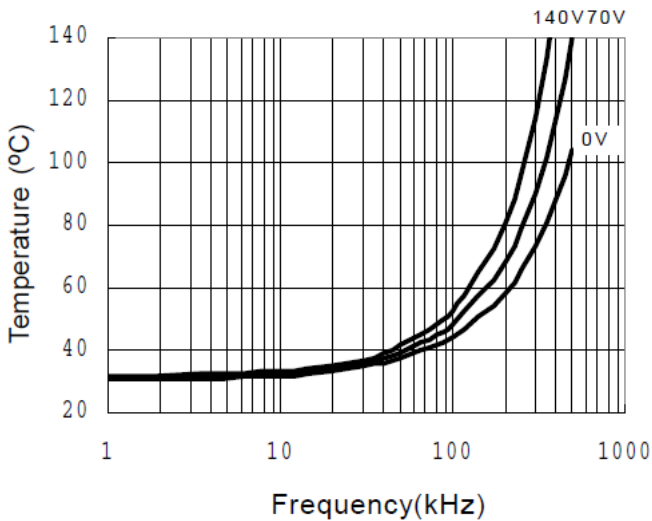
**Figure 28. IRS21864 vs. Frequency (IRFPE50)**  
 $R_{gate} = 10\Omega$ ,  $V_{CC} = 15V$



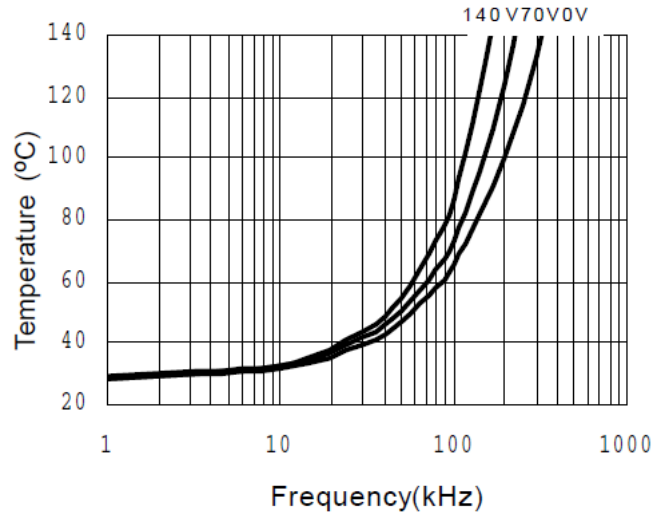
**Figure 29. IRS2186S vs. Frequency (IRFBC20)**  
 $R_{gate} = 33\Omega, V_{CC} = 15V$



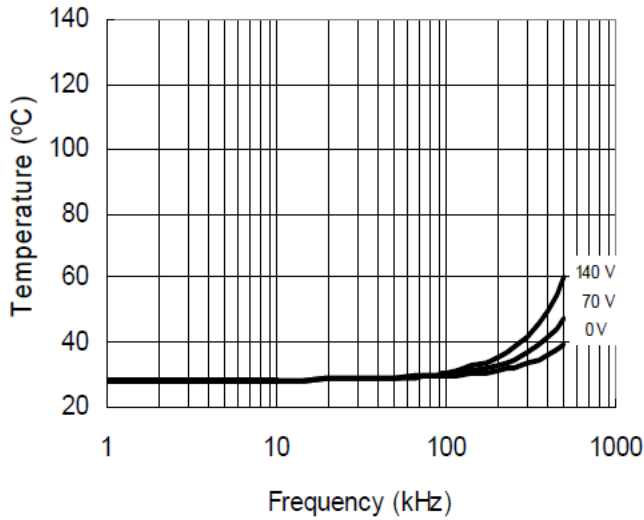
**Figure 30. IRS2186S vs. Frequency (IRFBC30)**  
 $R_{gate} = 22\Omega, V_{CC} = 15V$



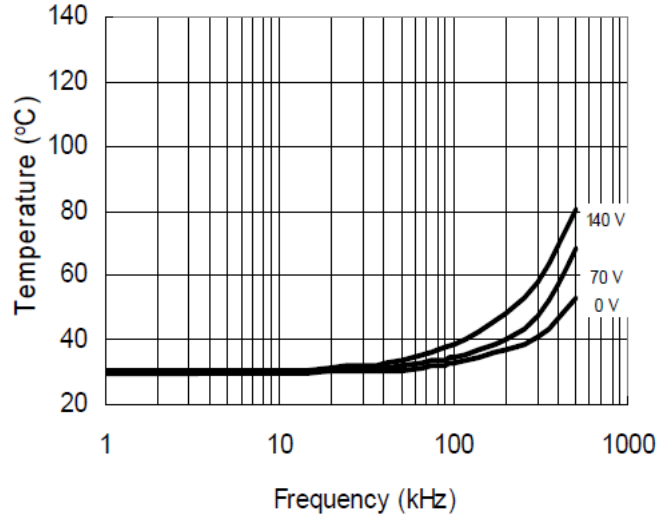
**Figure 31. IRS2186S vs. Frequency (IRFBC40)**  
 $R_{gate} = 15\Omega, V_{CC} = 15V$



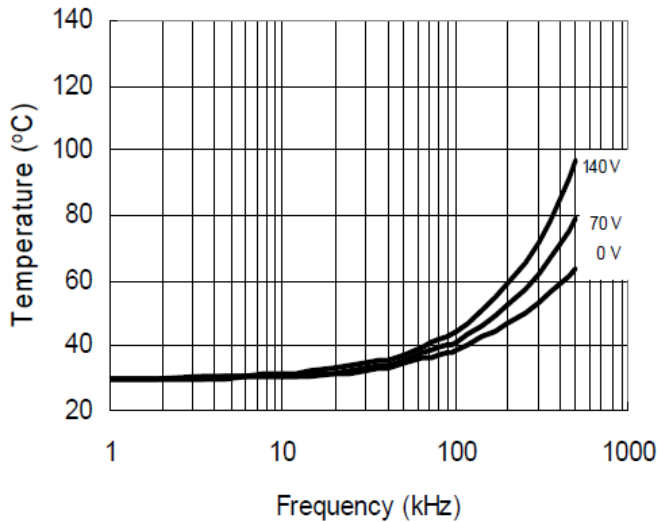
**Figure 32. IRS2186S vs. Frequency (IRFPE50)**  
 $R_{gate} = 10\Omega, V_{CC} = 15V$



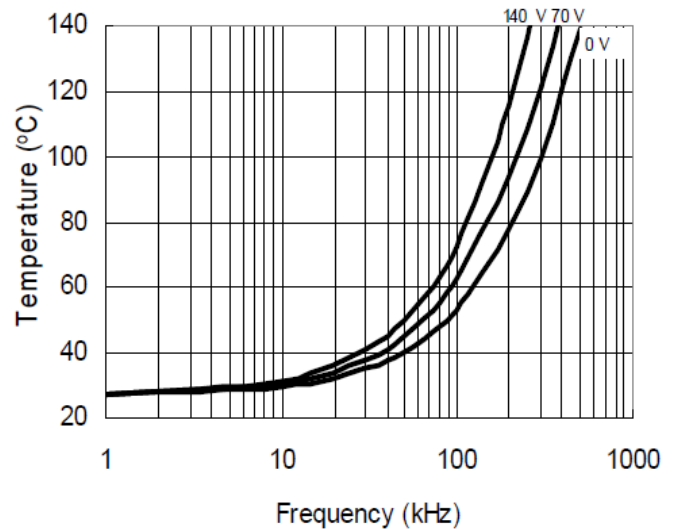
**Figure 33. IRS21864S vs. Frequency (IRFBC20)**  
 $R_{gate} = 33\Omega, V_{CC} = 15V$



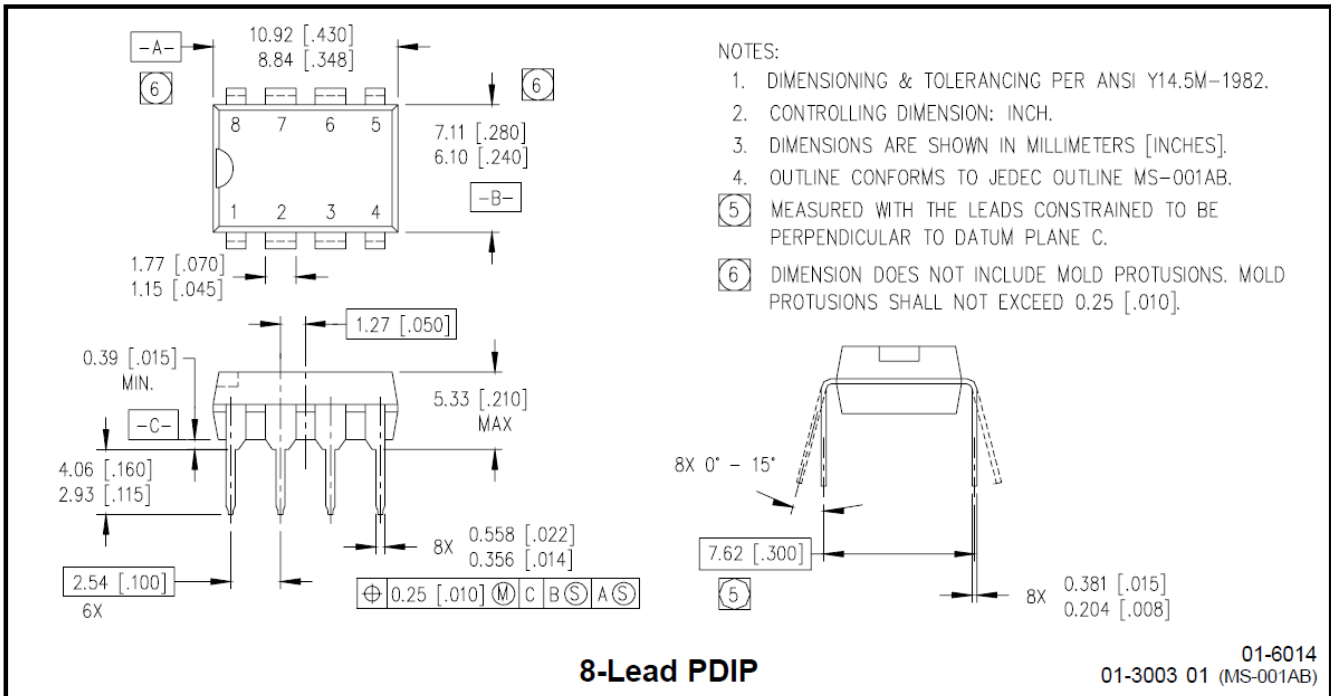
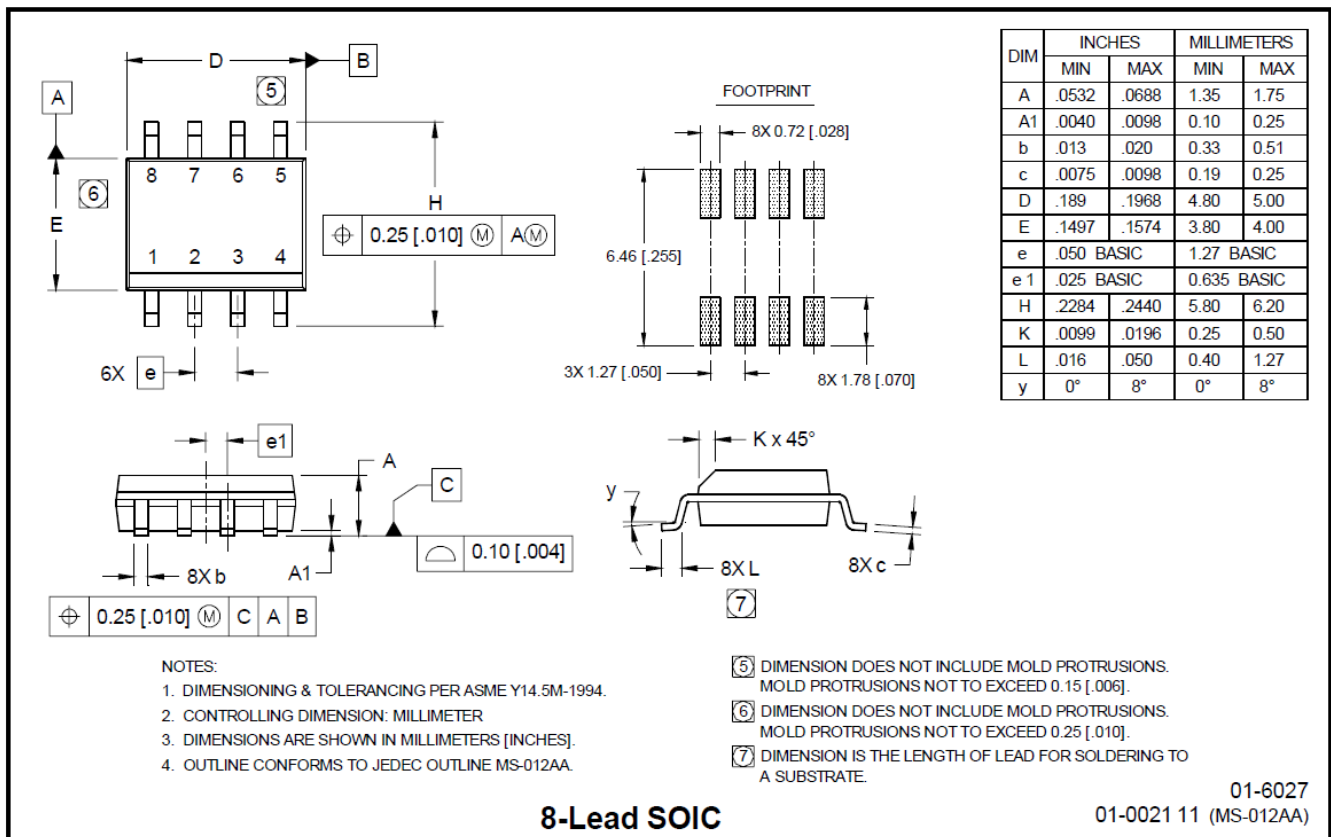
**Figure 34. IRS21864S vs. Frequency (IRFBC30)**  
 $R_{gate} = 22\Omega, V_{CC} = 15V$

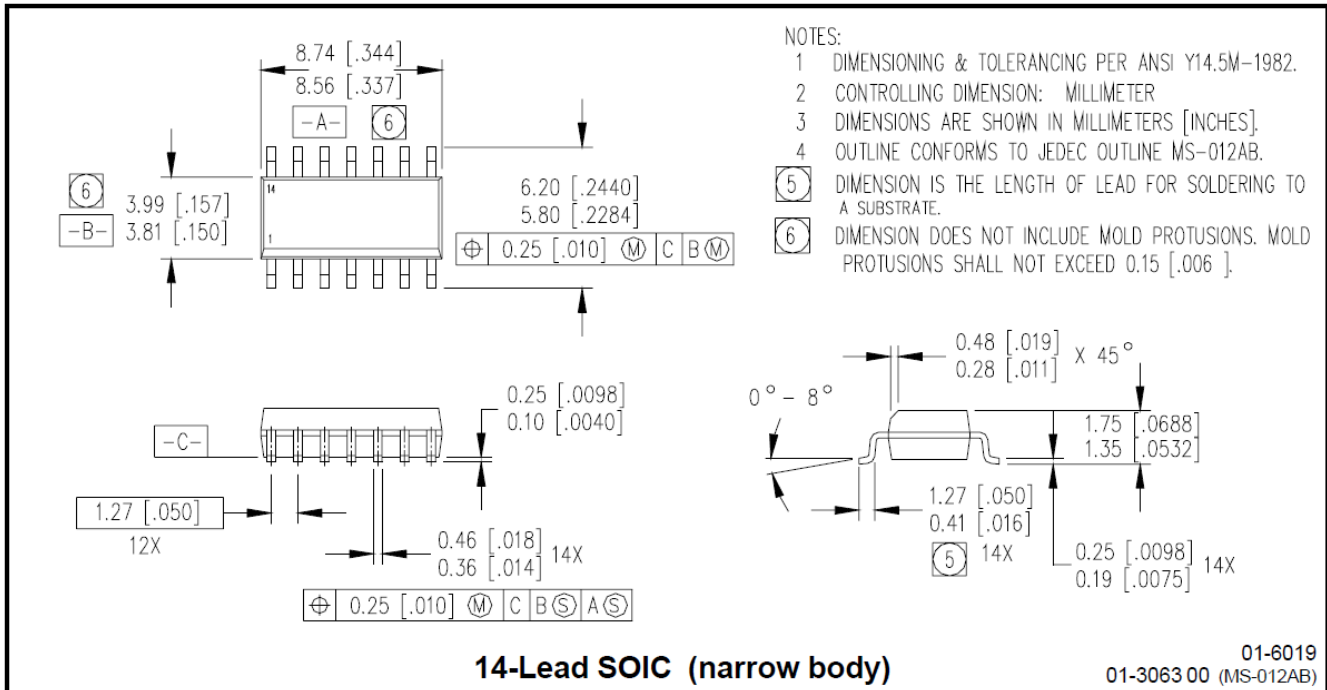
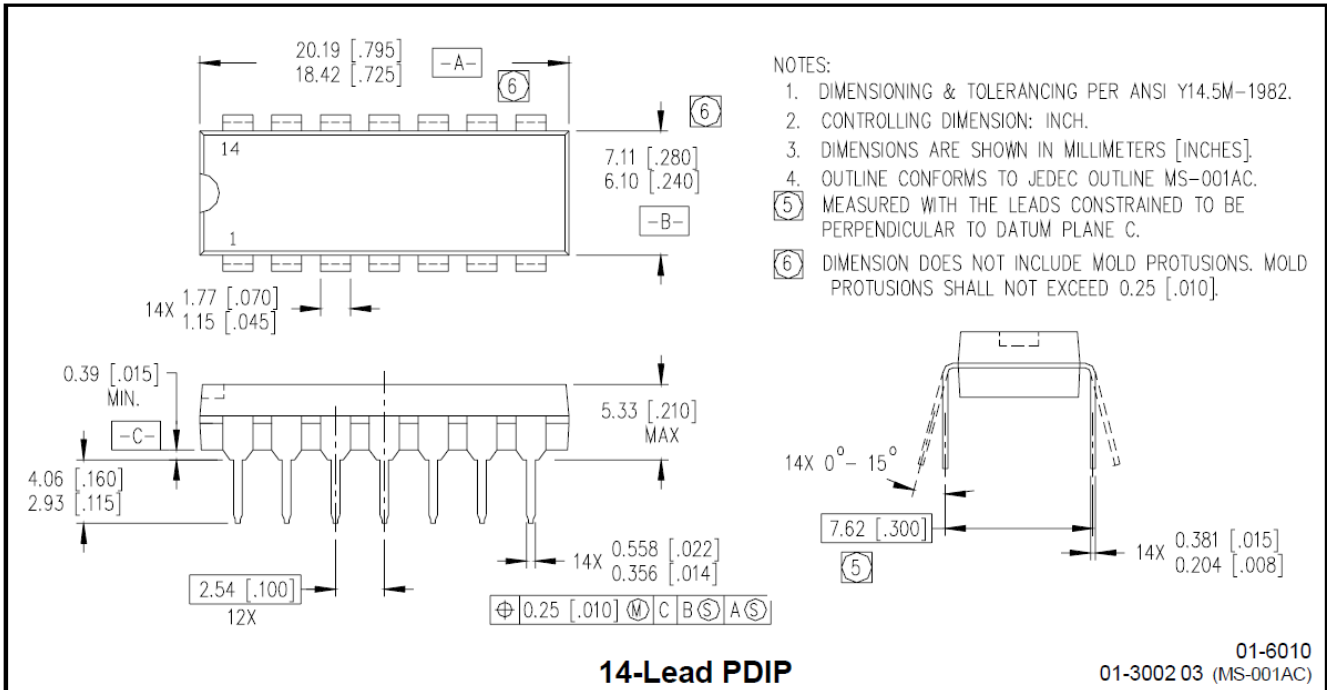


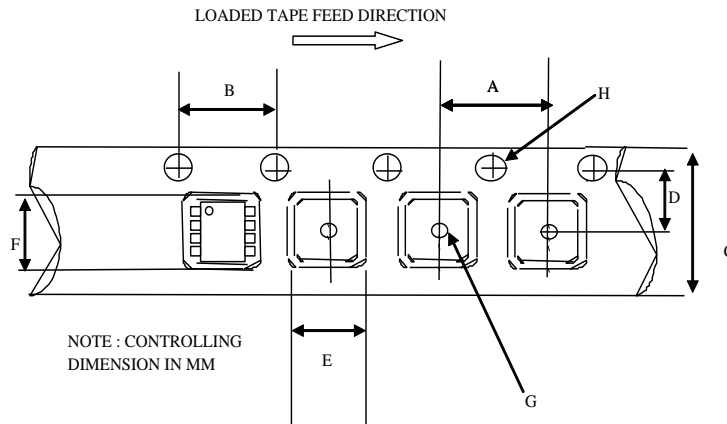
**Figure 35. IRS21864S vs. Frequency (IRFBC40)**  
 $R_{gate} = 15\Omega, V_{CC} = 15V$



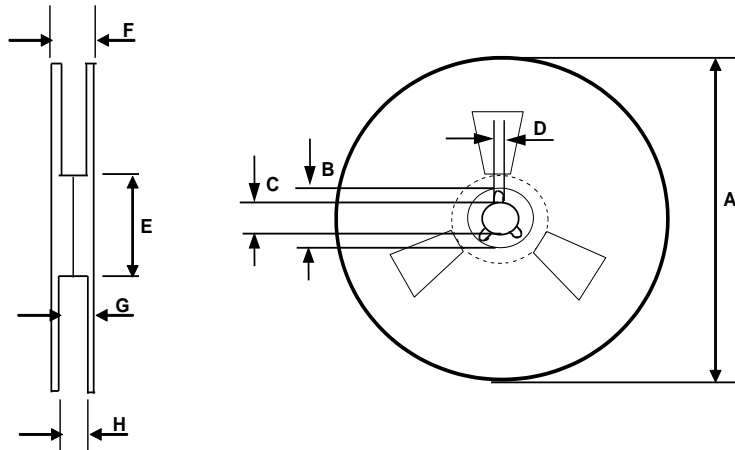
**Figure 36. IRS21864S vs. Frequency (IRFPE50)**  
 $R_{gate} = 10\Omega, V_{CC} = 15V$

**Package Details: PDIP8, SO8N**

**8-Lead PDIP**

**8-Lead SOIC**

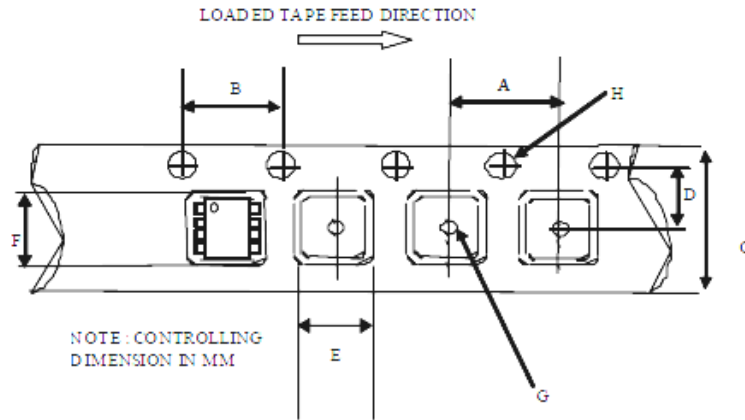
**Package Details: PDIP14, SO14N**


**Tape and Reel Details: SO8N**

**CARRIER TAPE DIMENSION FOR 8SOICN**

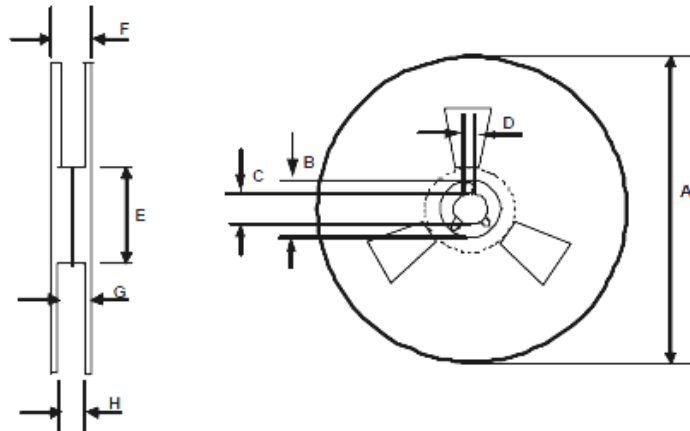
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062


**REEL DIMENSIONS FOR 8SOICN**

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

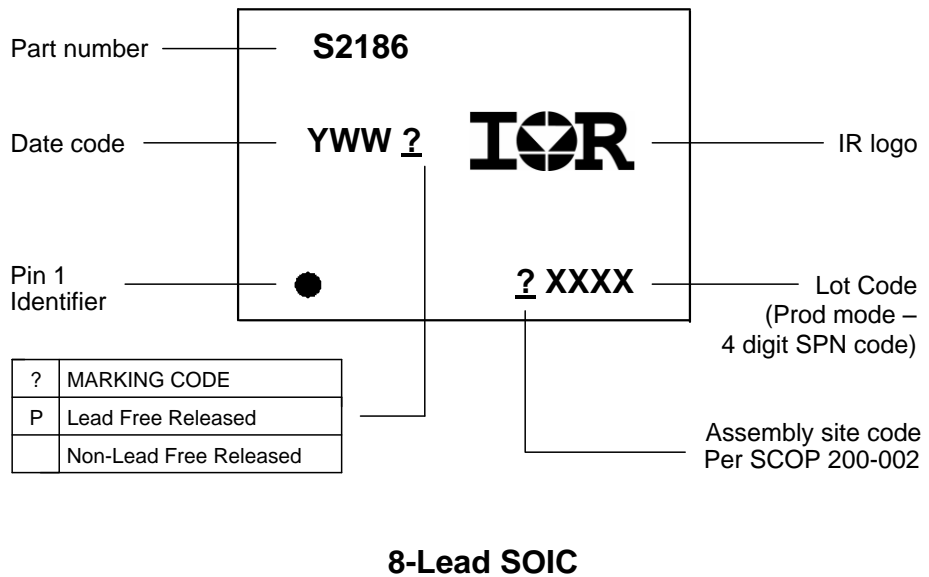
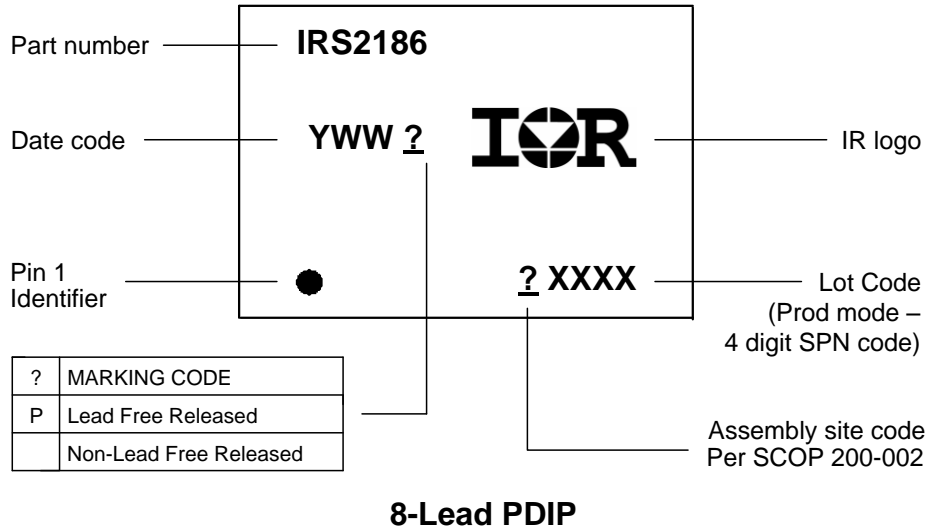
**Tape and Reel Details: SO14N**

**CARRIER TAPE DIMENSION FOR 14SO1CN**

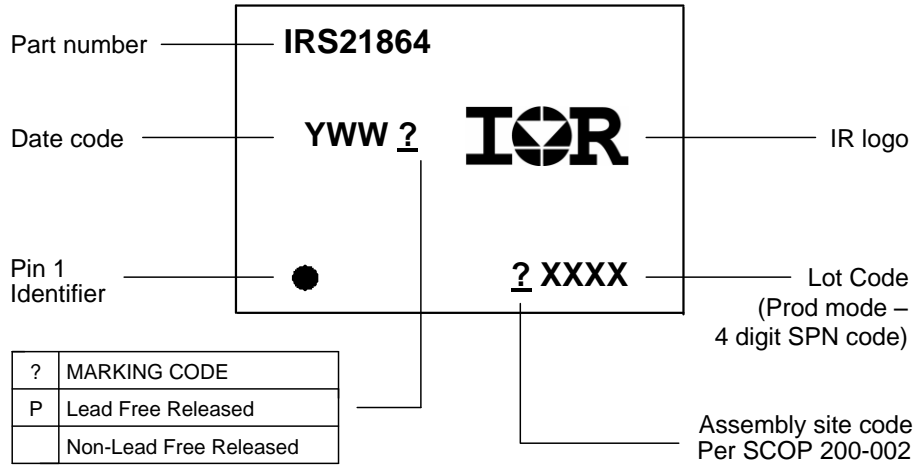
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B 3	.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	9.40	9.60	0.370	0.378
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062


**REEL DIMENSIONS FOR 14SO1CN**

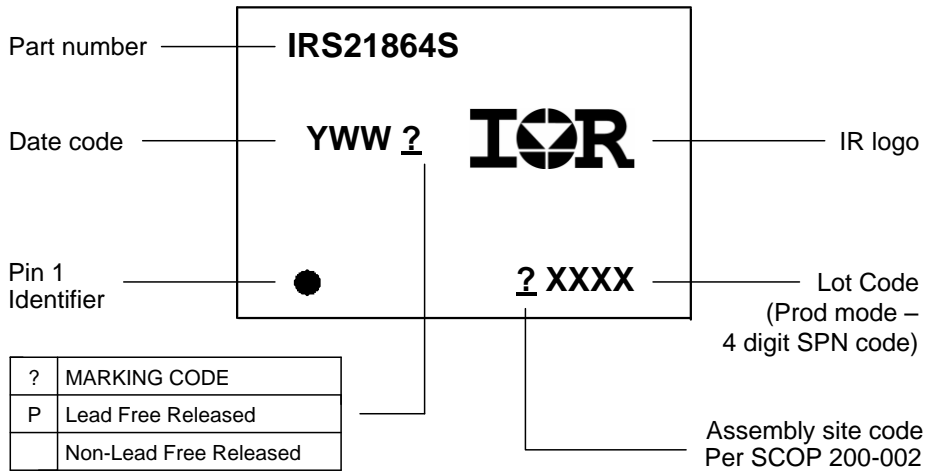
Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

**Part Marking Information**





**14-Lead PDIP**



**14-Lead SOIC**

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Industrial <sup>††</sup> (per JEDEC JESD 47)	
	Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
<b>Moisture Sensitivity Level</b>	SOIC8N	MSL2 <sup>†††</sup> (per IPC/JEDEC J-STD 020)
	PDIP8	Not applicable (non-surface mount package style)
	SOIC14N	MSL2 <sup>†††</sup> (per IPC/JEDEC J-STD 020)
	PDIP14	Not applicable (non-surface mount package style)
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

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