THE DATASHEET OF

TPS25961DRVR

TPS25961 2.7-V–19-V, 106-mΩ, eFuse With Adjustable Current Limit and Short-Circuit Protection

1 Features

- Wide input voltage range: 2.7 V to 19 V
  - 21-V absolute maximum
- Low on-resistance: Ron = 106 -mΩ (typical)
- Active high enable input with adjustable undervoltage lockout (UVLO)
- Overvoltage protection with a response time of 1.3 µs (typical)
  - Fixed internal threshold: 5.98 V (typical)
  - Adjustable threshold using external resistor divider
- Overcurrent protection:
  - Adjustable current limit threshold: 0.1 A to 2 A
  - Current limit accuracy:
    - ±20% (typical) across current range
    - ±18% (maximum) at 1.45-A current limit, T_A = 25°C
- Short-circuit protection with a response time of 5 µs (typical)
- Output slew rate control (dVdt): 5.17 V/ms (typical)
- Overtemperature protection (OTP)
- Auto-retry after fault
- Low quiescent current: 130 µA (typical)
- UL 2367 recognition (pending)
- IEC 62368 CB certification (pending)
- Small footprint: 2 mm × 2 mm SON package

2 Applications

- Adapter input protection
- Energy meters
- Smart speakers
- Wireless Earbud chargers
- Set-top boxes
- IP network cameras

3 Description

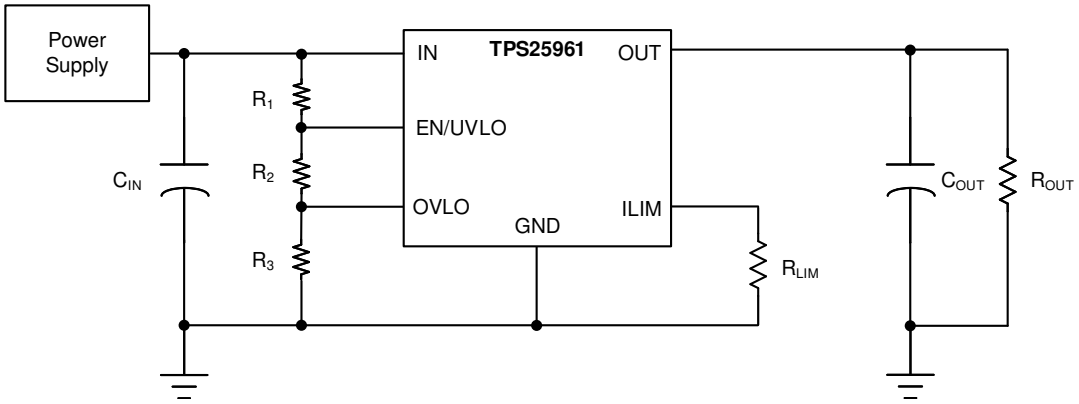
The TPS25961 *eFuse* (integrated FET hot-swap device) is a highly integrated circuit protection and power management solution in a small package. The device provides multiple protection modes using very few external components and is a robust defense against overloads, short-circuits, voltage surges, and excessive inrush current. Output current limit level can be set with a single external resistor. Inrush current is managed using output slew rate control internally. To protect an input overvoltage condition, the device provides an option to externally set a user-defined overvoltage cutoff threshold or use a fixed internal threshold.

The devices are characterized for operation over a junction temperature range of –40 °C to +125 °C.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
TPS25961DRV	SON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2022	*	Initial Release

5 Pin Configuration and Functions

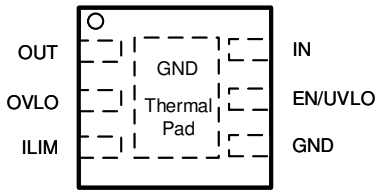


Figure 5-1. DRV Package, 6-Pin SON (Top View)

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1	Power	Power output.
OVLO	2	Analog Input	An external resistor divider from supply rail can be used to adjust the overvoltage lockout threshold. Connect to GND directly to use internal fixed overvoltage lockout threshold. **Do not leave floating.**
ILIM	3	Analog Output	An external resistor from this pin to GND sets the output current limit threshold. Leave it open to set the current limit threshold to minimum value.
GND	4	Ground	Connect to system electrical ground.
EN/UVLO	5	Analog Input	Active High Enable for the device. A resistor divider from supply rail can be used to adjust the undervoltage lockout threshold. **Do not leave floating.**
IN	6	Power	Power input.
GND	PAD	Thermal/ Ground	The exposed pad is used primarily for heat dissipation and must be connected to GND plane on the PCB.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Maximum input voltage range, –40°C ≤ T_J ≤ 125°C	IN	–0.3	21	V
V_{OUT}	Maximum output voltage range, –40°C ≤ T_J ≤ 125°C	OUT	–0.3	V_{IN} + 0.3	
$V_{EN/UVLO}$	Maximum EN/UVLO pin voltage range	EN/UVLO	–0.3	20	V
V_{OV}	Maximum OVLO pin voltage range	OVLO	–0.3	6.5	V
V_{ILIM}	Maximum ILIM pin voltage range	ILIM	Internally limited		V
I_{MAX}	Maximum continuous switch current	IN to OUT	Internally limited		A
T_J	Junction temperature		Internally limited		°C
T_{LEAD}	Maximum lead temperature			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Input voltage range	IN	2.7	19	V
V_{OUT}	Output voltage range	OUT		V_{IN}	V
$V_{EN/UVLO}$	EN/UVLO pin voltage range	EN/UVLO		5(1)	V
V_{OV}	OVLO pin voltage range	OVLO	0.5	1.5	V
R_{ILIM}	ILIM pin resistance to GND	ILIM	25		kΩ
I_{MAX}	Continuous switch current, T_J ≤ 125°C	IN to OUT		2	A
T_J	Junction temperature		–40	125	°C

(1) For supply voltages below 5V, it is okay to pull up the EN pin to IN directly. For supply voltages greater than 5V , it is recommended to use a resistor divider with minimum pull-up resistor value of 350 kΩ.

6.4 Thermal Information

THERMAL METRIC (1) (2)		TPS25961 DRV (SON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.1	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	80.4	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	16.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	38.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Based on simulations conducted with the device mounted on a custom 4-layer PCB (2s2p)

6.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 1 V, ILIM = Open. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)					
$I_{Q(ON)}$	IN supply quiescent current		130	165	µA
$I_{Q(OFF)}$	IN supply OFF state current ($V_{SD(F)}$ < V_{EN} < $V_{UVLO(F)}$)		144	230	µA
I_{SD}	IN supply shutdown current (V_{EN} < $V_{SD(F)}$)		0.6	1.5	µA
$V_{UVP(R)}$	IN supply UVP rising threshold	2.46	2.54	2.61	V
$V_{UVP(F)}$	IN supply UVP falling threshold	2.31	2.42	2.54	V
$V_{OVP(R)}$	VIN fixed overvoltage rising threshold, OVLO = GND, T_J = 25°C	5.55	5.98	6.5	V
V_{OVPHys}	VIN fixed overvoltage hysteresis, OVLO = GND	85	111	135	mV
OVERCURRENT PROTECTION (OUT)					
I_{LIM}	Overcurrent threshold, ILIM = Open, T_J = 25°C		0.116		A
	Overcurrent threshold, R_{ILIM} = 250 kΩ, T_J = 25°C		0.212		A
	Overcurrent threshold, R_{ILIM} = 100 kΩ, T_J = 25°C		0.516		A
	Overcurrent threshold, R_{ILIM} = 62.5 kΩ, T_J = 25°C		0.856		A
	Overcurrent threshold, R_{ILIM} = 34.48 kΩ, T_J = 25°C	1.189	1.45	1.711	A
	Overcurrent threshold, R_{ILIM} = 25 kΩ, T_J = 25°C		2.36		A
I_{SC}	Fast-trip threshold		8.25		A
ON RESISTANCE (IN - OUT)					
R_{ON}	2.7 ≤ V_{IN} < 4.5 V, I_{OUT} = 1 A, R_{ILIM} = 34.48 kΩ		132	240	mΩ
	4.5 ≤ V_{IN} ≤ 19 V, I_{OUT} = 1 A, R_{ILIM} = 34.48 kΩ		106	177	mΩ
	2.7 ≤ V_{IN} < 4.5 V, I_{OUT} = 0.1 A, R_{ILIM} = 100 kΩ, T_J = 25°C		243		mΩ
	4.5 ≤ V_{IN} ≤ 19 V, I_{OUT} = 0.1 A, R_{ILIM} = 100 kΩ, T_J = 25°C		195		mΩ
	2.7 ≤ V_{IN} < 4.5 V, I_{OUT} = 0.1 A, R_{ILIM} = 250 kΩ, T_J = 25°C		455		mΩ
	4.5 ≤ V_{IN} ≤ 19 V, I_{OUT} = 0.1 A, R_{ILIM} = 250 kΩ, T_J = 25°C		367		mΩ
	2.7 ≤ V_{IN} < 4.5 V, I_{OUT} = 0.05 A, ILIM = Open, T_J = 25°C		833		mΩ
	4.5 ≤ V_{IN} ≤ 19 V, I_{OUT} = 0.05 A, ILIM = Open, T_J = 25°C		702		mΩ
ENABLE/UNDERVOLTAGE LOCKOUT (EN/UVLO)					
$V_{UVLO(R)}$	EN/UVLO rising threshold	1.2	1.24	1.27	V
$V_{UVLO(F)}$	EN/UVLO falling threshold	1.1	1.132	1.16	V
$V_{SD(F)}$	EN/UVLO falling threshold for lowest shutdown current	0.6			V
I_{ENLKG}	EN/UVLO pin leakage current	-0.1		0.1	µA
OVERVOLTAGE LOCKOUT (OVLO)					
$V_{OVLO(R)}$	OVLO rising threshold	1.2	1.24	1.27	V
$V_{OVLO(F)}$	OVLO falling threshold	1.1	1.13	1.161	V
I_{OVLKG}	OVLO pin leakage current	-0.1		0.1	µA
OVERTEMPERATURE PROTECTION (OTP)					
TSD	Thermal Shutdown rising threshold, T_J↑		170		°C
TSD_{HYS}	Thermal Shutdown hysteresis, T_J↓		30		°C

6.6 Timing Requirements

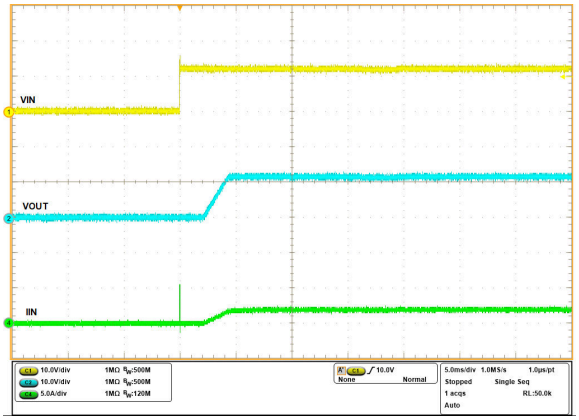
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVLO}	Overvoltage lock-out response time	V_{OVLO} > $V_{OV(R)}$ to V_{OUT}↓		1.3		µs
t_{LIM}	Current limit response time	I_{OUT} > 1.5 × I_{LIM} to I_{OUT} within 5% of I_{LIM}		30		µs
t_{SC}	Short-circuit response time	I_{OUT} > I_{SC} to output current cut off		5		µs
$t_{TSD,RST}$	Thermal Shutdown auto-retry Interval	Device enabled and T_J < TSD – TSD_{HYS}		110		ms

6.7 Switching Characteristics

The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As C_{dVdt} is increased it will slow the rising slew rate (SR). See Slew Rate and Inrush Current Control (dVdt) section for more details. The Turn-Off Delay and Fall Time, however, are dependent on the RC time constant of the load capacitance (C_{OUT}) and Load Resistance (R_L). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady state condition and the load voltage is completely discharged before the device is enabled. Typical values are taken at T_J = 25°C unless specifically noted otherwise. R_L = 100 Ω, C_{OUT} = 1 µF.

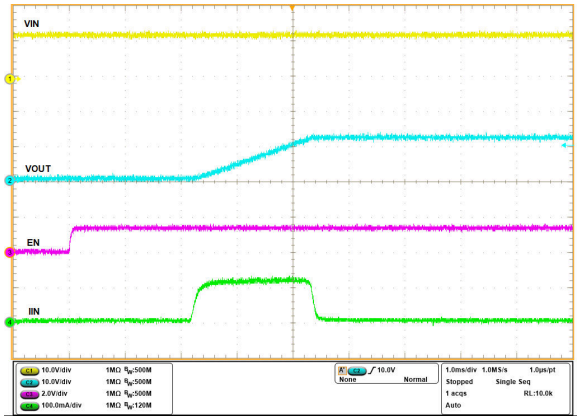
PARAMETER		V_{IN}	Typ	UNITS
SR_{ON}	Output rising slew rate	3.3 V	4.43	V/ms
		12 V	5.17	
		18 V	5.19	
$t_{D,ON}$	Turn on delay	3.3 V	2.14	ms
		12 V	2.37	
		18 V	2.50	
t_R	Rise time	3.3 V	0.58	ms
		12 V	1.83	
		18 V	2.67	
t_{ON}	Turn on time	3.3 V	2.71	ms
		12 V	4.2	
		18 V	5.17	
$t_{D,OFF}$	Turn off delay	3.3 V	15.00	µs
		12 V	14.22	
		18 V	12.44	

6.8 Typical Characteristics



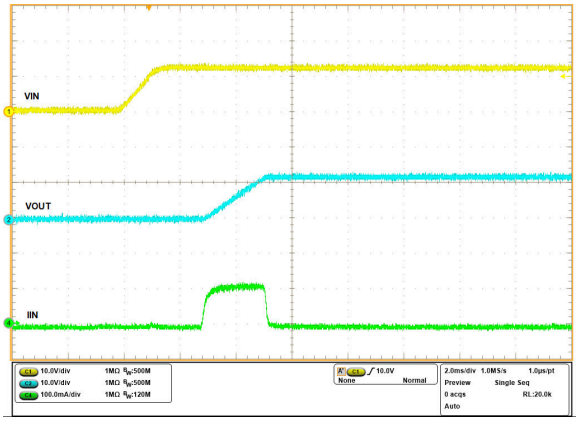
C_{OUT} = 22 µF, R_{OUT} = 6 Ω, IN hot-plugged to 12 V

Figure 6-1. Input Hotplug Response



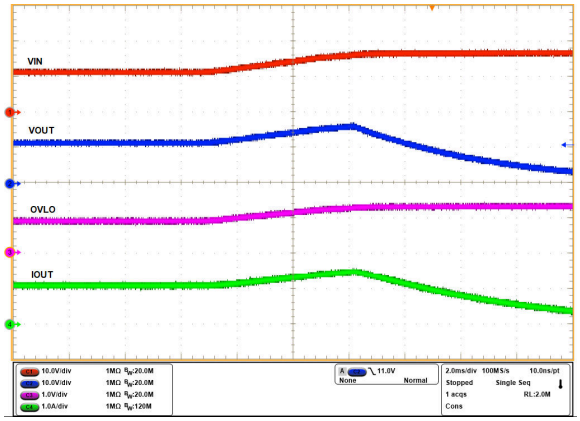
V_{IN} = 12 V, C_{OUT} = 22 µF, EN pin stepped up from 0 V to 1.5 V

Figure 6-2. Power Up Using Enable Pin



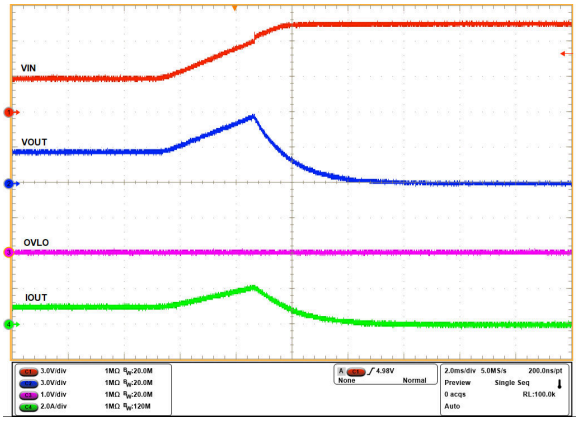
C_{OUT} = 22 µF, EN pin held High, V_{IN} ramped up to 12 V

Figure 6-3. Power Up Using Input Supply



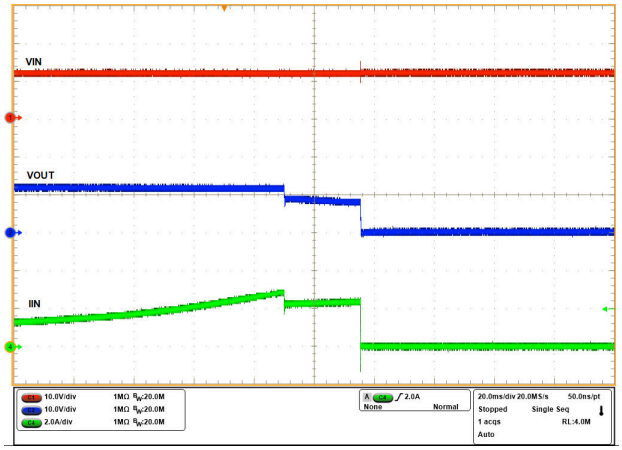
OVLO threshold set to 16 V using resistor ladder from VIN to GND, C_{OUT} = 470 µF, R_{OUT} = 12 Ω, V_{IN} increased from 10 V to 17 V

Figure 6-4. Overvoltage Lockout Response - Adjustable Threshold



OVLO pin shorted to GND, C_{OUT} = 470 µF, R_{OUT} = 3.3 Ω, V_{IN} increased from 2.7 V to 7.5 V

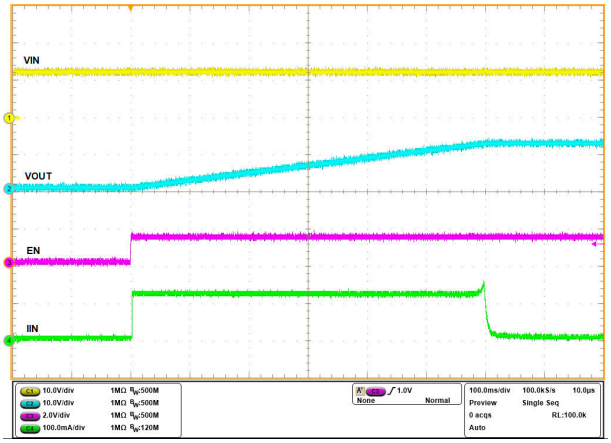
Figure 6-5. Overvoltage Lockout Response - Internal Fixed Threshold



V_{IN} = 12 V, R_{ILIM} = 25 kΩ, load currently gradually ramped up above 2.5 A

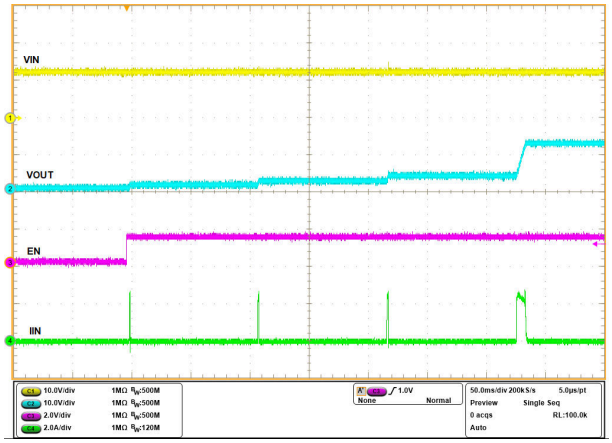
Figure 6-6. Current Limit Followed by Thermal Shutdown

6.8 Typical Characteristics (continued)



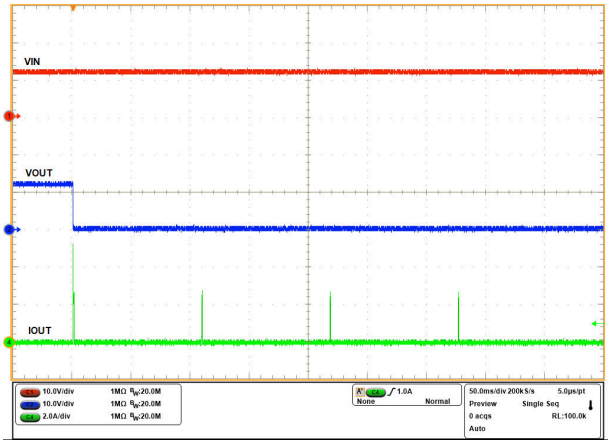
V_{IN} = 12 V, C_{OUT} = 6400 µF, R_{OUT} = Open, R_{ILIM} = Open, EN pin toggled from Low to High

Figure 6-7. Charging Up Large Capacitor Using Low Current Limit Setting



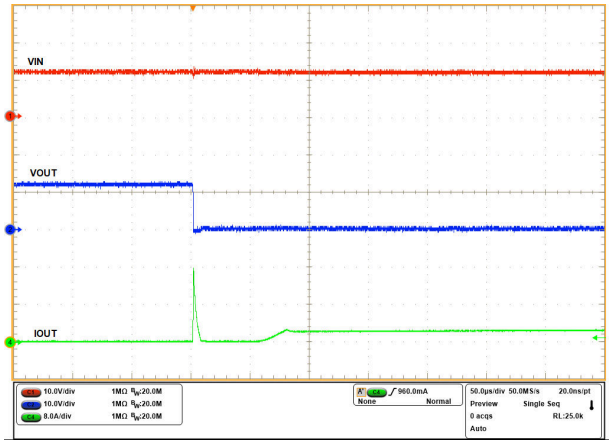
V_{IN} = 12 V, C_{OUT} = 2200 µF, R_{OUT} = Open, R_{ILIM} = 25 kΩ, EN pin toggled from Low to High

Figure 6-8. Charging Up Large Capacitor Using High Current Limit Setting - Hiccup Mode



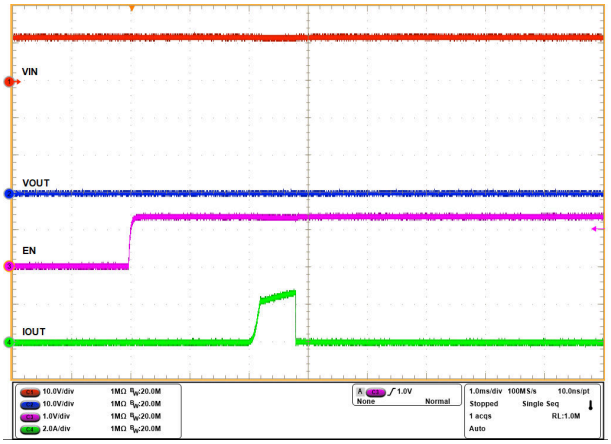
V_{IN} = 12 V, R_{ILM} = 25 kΩ, OUT pin shorted to GND

Figure 6-9. Output Short-Circuit While ON



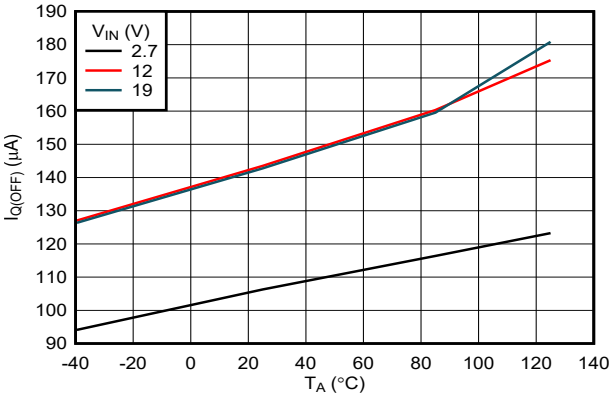
V_{IN} = 12 V, R_{ILM} = 25 kΩ, OUT pin shorted to GND

Figure 6-10. Short-Circuit While ON (Zoomed In)



V_{IN} = 12 V, R_{ILM} = 25 kΩ, EN pin toggled from Low to High with OUT pin shorted to GND

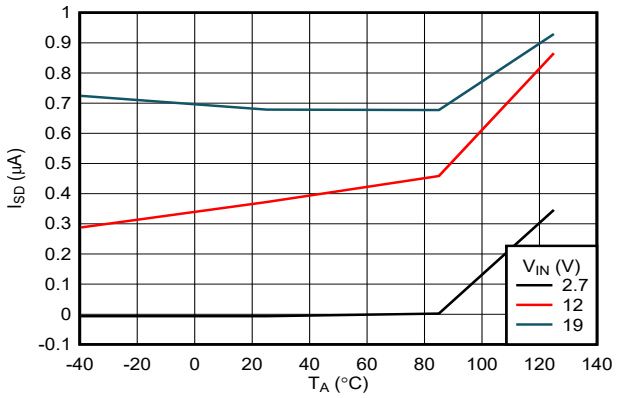
Figure 6-11. Power Up Into Short-Circuit



EN/UVLO pin voltage > $V_{UVLO(R)}$

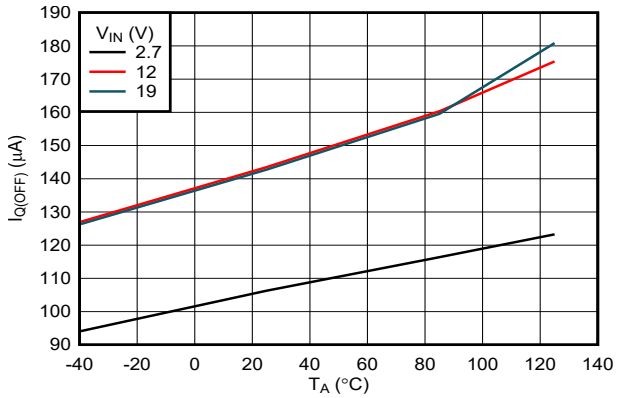
Figure 6-12. Steady State Quiescent Current vs Temperature

6.8 Typical Characteristics (continued)



EN/UVLO pin voltage < $V_{SD(F)}$

Figure 6-13. Shutdown Current vs Temperature



$V_{SD(F)}$ < EN/UVLO pin voltage < $V_{UVLO(F)}$

Figure 6-14. OFF state Current vs Temperature

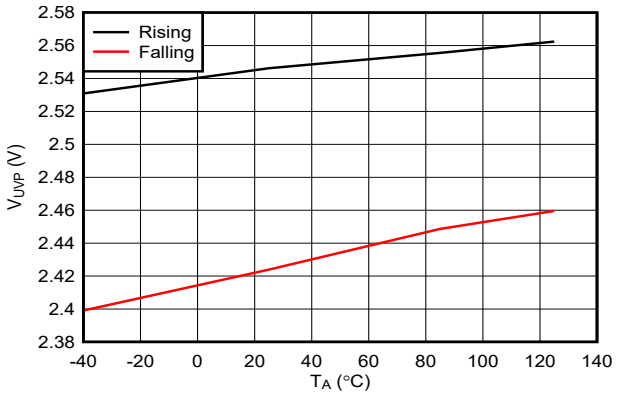


Figure 6-15. IN Supply Undervoltage Threshold vs Temperature

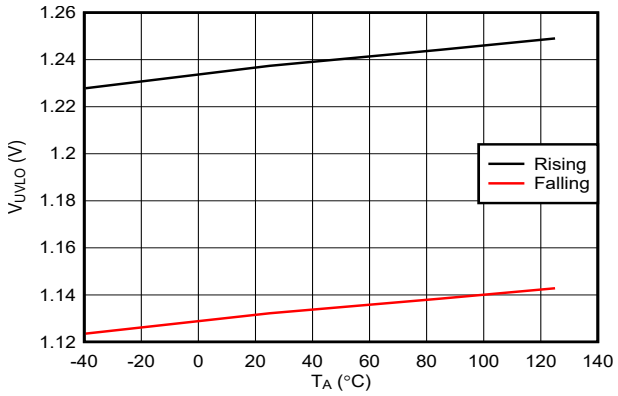


Figure 6-16. EN/UVLO Pin Threshold for FET ON/OFF Control vs Temperature

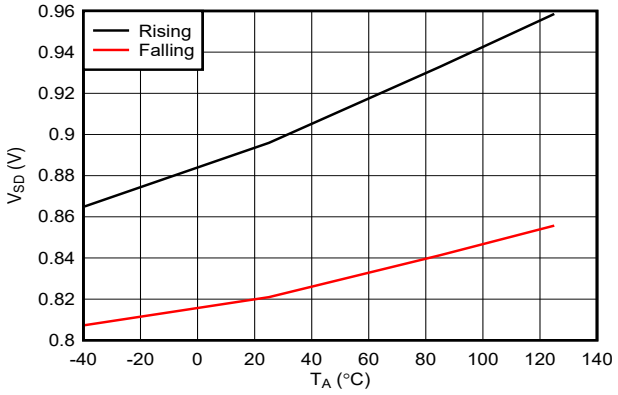


Figure 6-17. EN/UVLO Pin Threshold for Lowest Shutdown Current vs Temperature

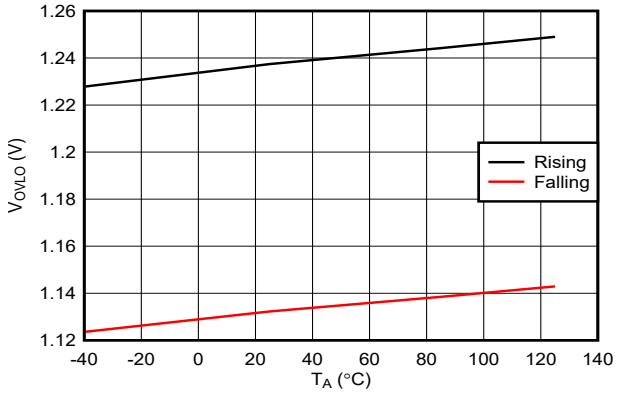


Figure 6-18. OVLO Pin Threshold vs Temperature

6.8 Typical Characteristics (continued)

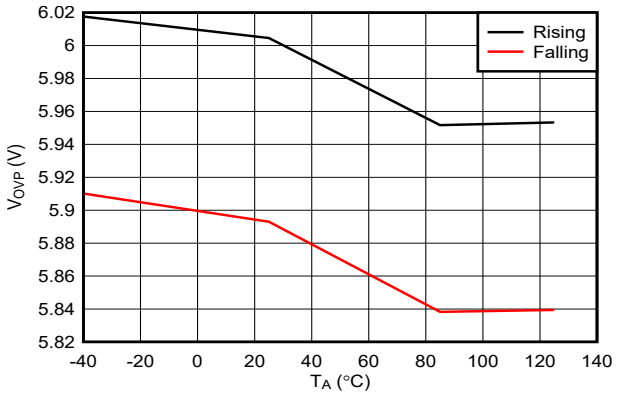
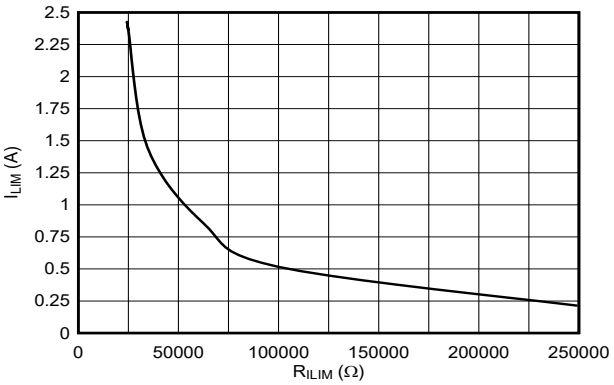
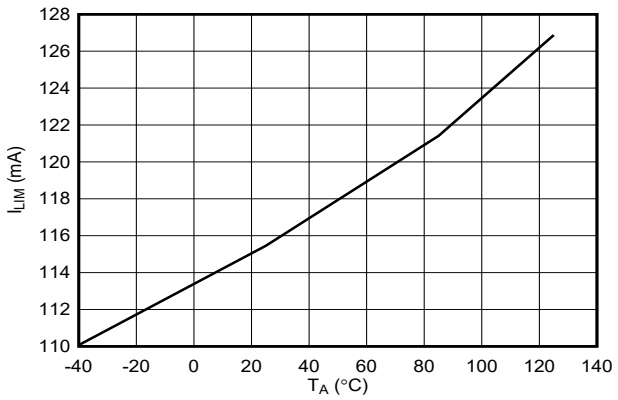


Figure 6-19. Internal Fixed Overvoltage Threshold vs Temperature



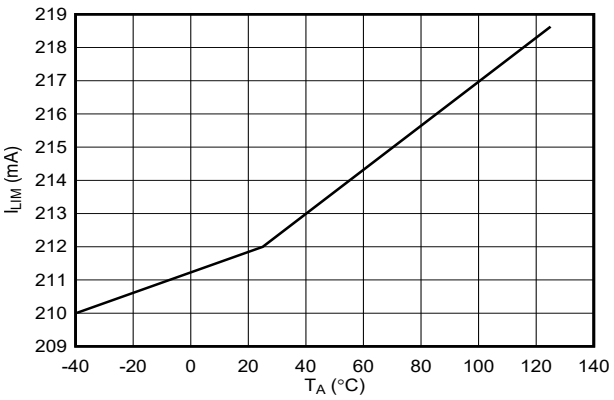
Applicable for I_{LIM} > 0.2 A, refer to this section for additional considerations.

Figure 6-20. Current Limit Threshold vs ILIM Resistor



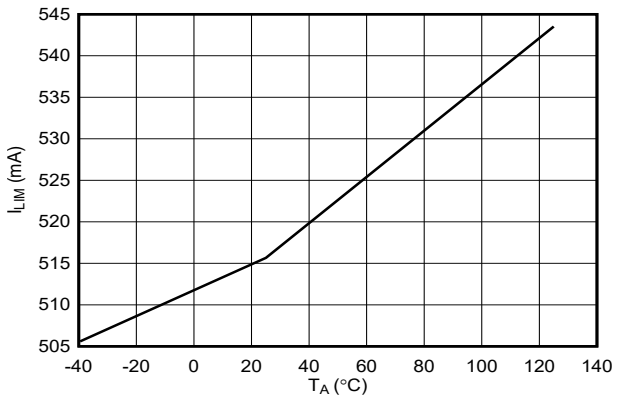
ILIM Pin Open

Figure 6-21. Current Limit Threshold vs Temperature



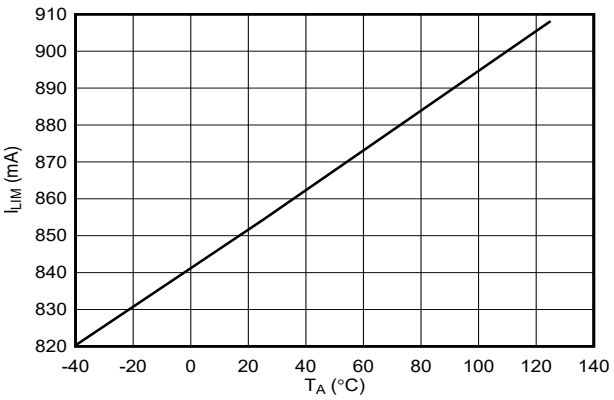
R_{ILIM} = 250 kΩ

Figure 6-22. Current Limit Threshold vs Temperature



R_{ILIM} = 100 kΩ

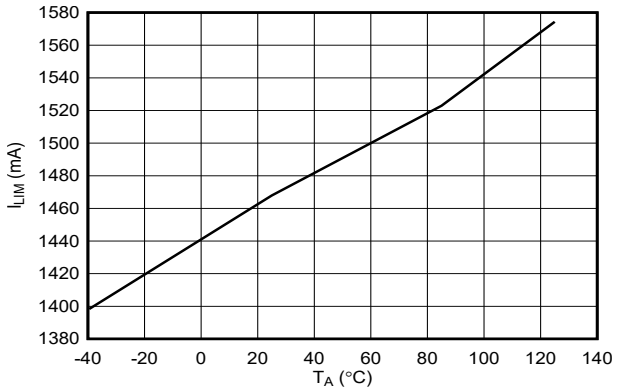
Figure 6-23. Current Limit Threshold vs Temperature



R_{ILIM} = 62.5 kΩ

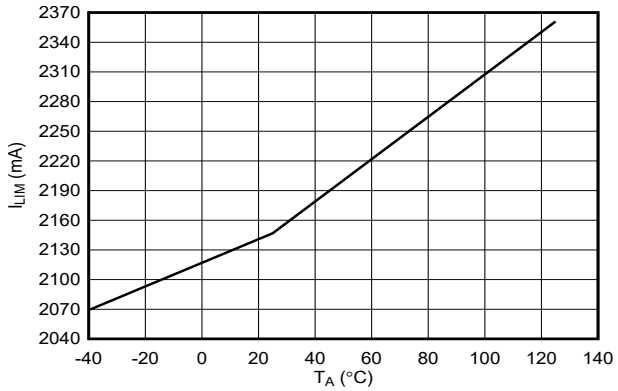
Figure 6-24. Current Limit Threshold vs Temperature

6.8 Typical Characteristics (continued)



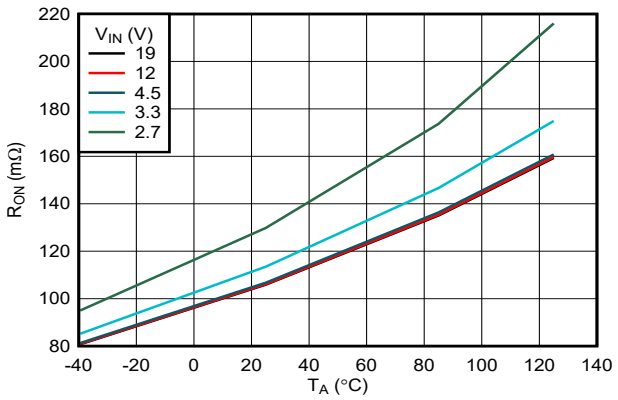
R_{ILIM} = 34.48 kΩ

Figure 6-25. Current Limit Threshold vs Temperature



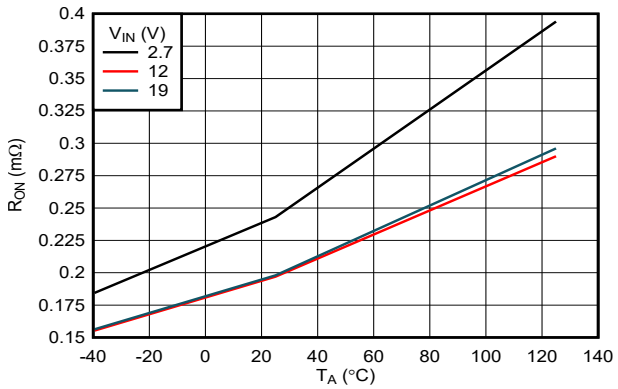
R_{ILIM} = 25 kΩ

Figure 6-26. Current Limit Threshold vs Temperature



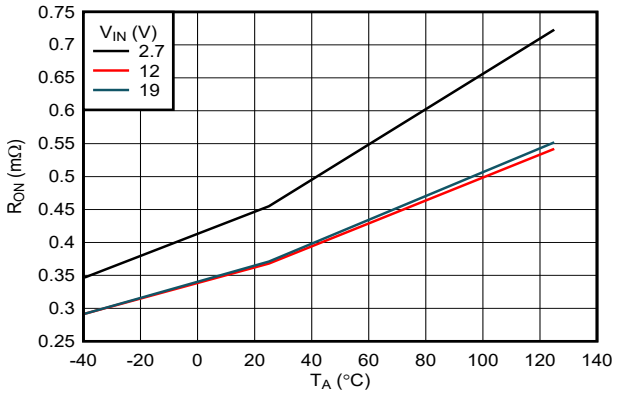
R_{ILIM} < 58.8 kΩ

Figure 6-27. ON Resistance vs Temperature



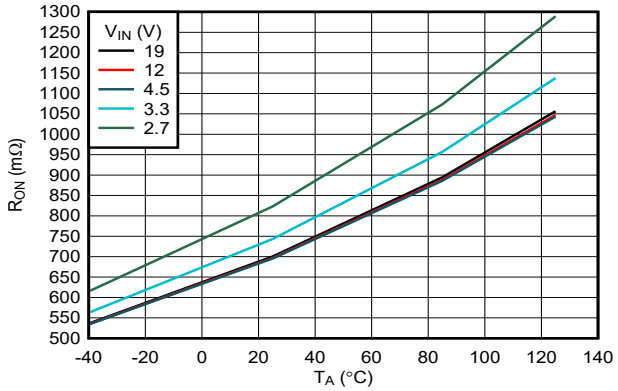
66.7 kΩ < R_{ILIM} < 111 kΩ

Figure 6-28. ON Resistance vs Temperature



142 kΩ < R_{ILIM} < 250 kΩ

Figure 6-29. ON Resistance vs Temperature



R_{ILIM} > 500 kΩ

Figure 6-30. ON Resistance vs Temperature

6.8 Typical Characteristics (continued)

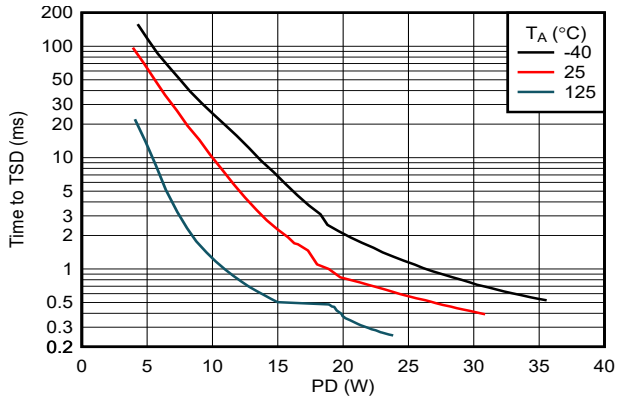


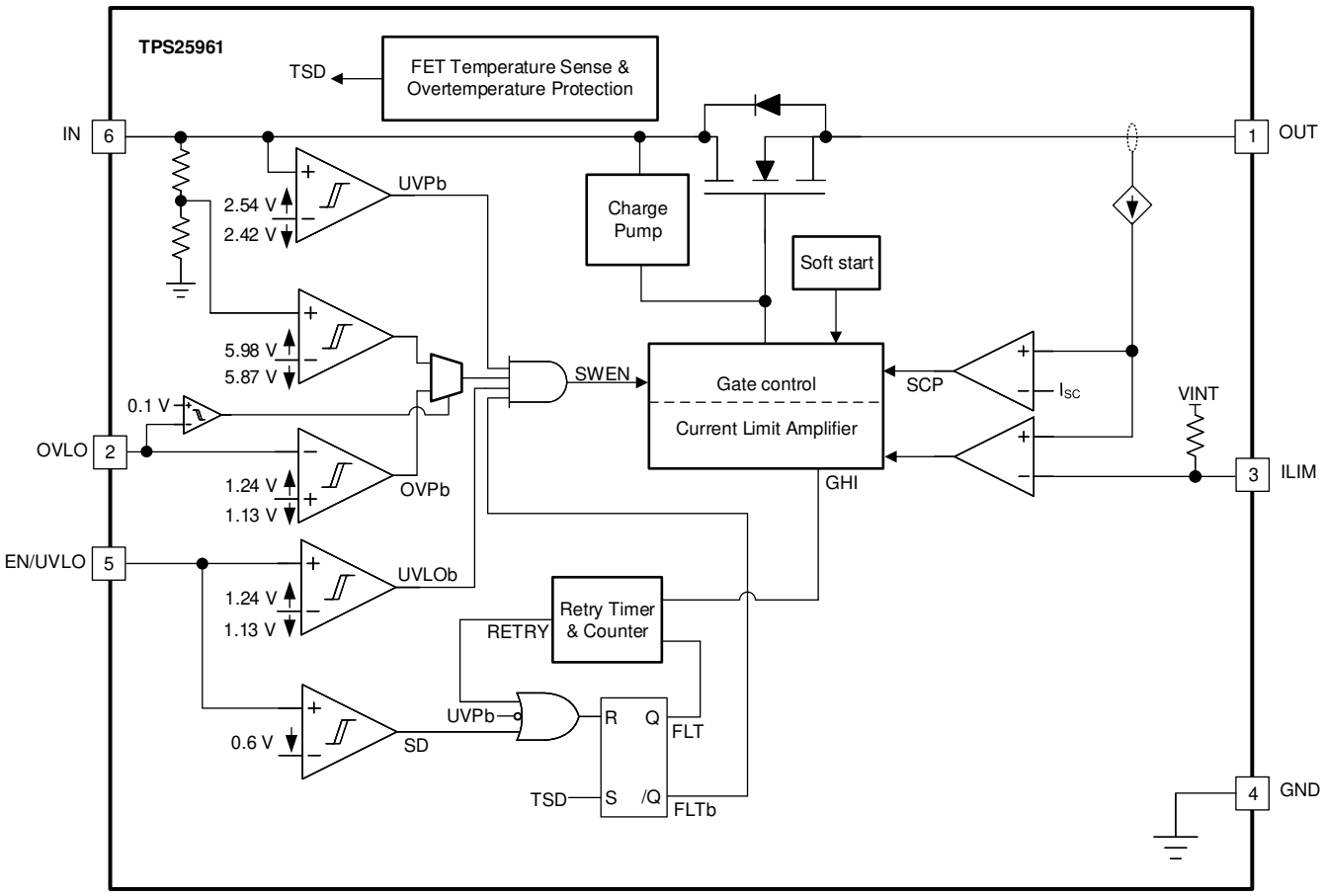
Figure 6-31. Time to Thermal Shutdown vs Power Dissipation

7 Detailed Description

7.1 Overview

The TPS25961 is an integrated eFuse device that is used to manage load voltage and load current. The device provides various factory programmed settings and user manageable settings, which allow device configuration for handling different transient and steady state supply and load fault conditions, thereby protecting the input supply and the downstream circuits connected to the device. The device also uses an in-built thermal shutdown mechanism to protect itself during these fault events.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Protection (UVP) and Undervoltage Lockout (UVLO)

TPS25961 constantly monitors the input supply to ensure that the load is powered up only when the voltage is at a sufficient level. During the start-up condition, the device waits for the input supply to rise above an internal fixed threshold $V_{UVP(R)}$ before it proceeds to turn ON the FET. Similarly, during the ON condition, if the input supply falls below the UVP threshold $V_{UVP(F)}$, the FET is turned OFF. The UVP rising and falling thresholds are slightly different, thereby providing some hysteresis and ensuring stable operation around the threshold voltage.

The TPS25961 also provides an user adjustable UVLO mechanism to ensure that the load is powered up only when the voltage is at a sufficient level as per the specific system requirement. This can be achieved by dividing the input supply and feeding it to the EN/UVLO pin. Whenever the voltage at the EN/UVLO pin falls below a threshold $V_{UVLO(F)}$, the device turns OFF the FET. The FET is turned ON again when the voltage rises above the threshold $V_{UVLO(R)}$. The rising and falling thresholds on this pin are slightly different, thereby providing some hysteresis and ensuring stable operation around the threshold voltage.

The user must choose the resistor divider values appropriately to map the desired input undervoltage level to the UVLO threshold of the part.

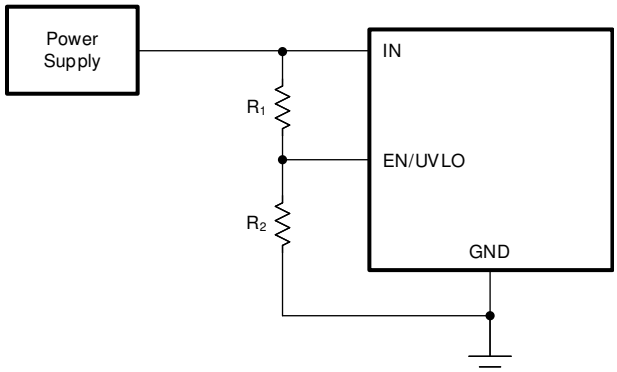


Figure 7-1. Adjustable Undervoltage Lockout

The equation below shows the calculations for the resistor divider values to be used to set the UVLO set-point for a given voltage supply.

$$VIN(UV) = VUVLO(F) \times \frac{R1 + R2}{R2} \quad (1)$$

7.3.2 Overvoltage Protection

The TPS25961 implements Overvoltage Protection on V_{IN} in case the applied voltage becomes too high for the system or device to properly operate. The Overvoltage Protection has a default lockout threshold of V_{OVP} , which is achieved by connecting the OVLO pin to GND.

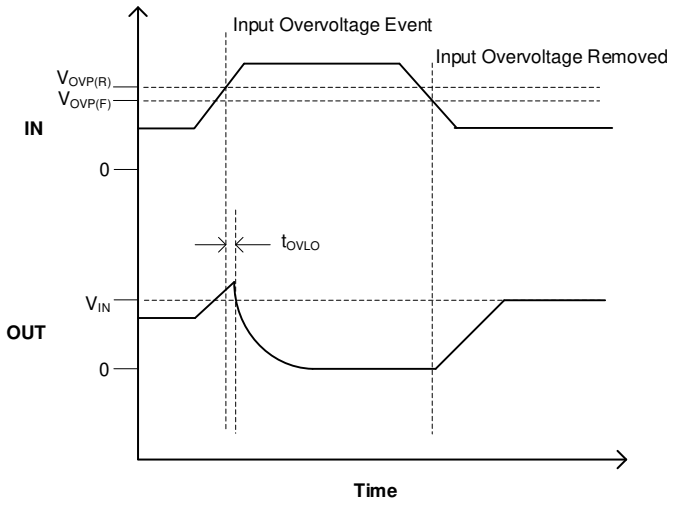


Figure 7-2. TPS25961 Fixed Overvoltage Lockout Response

It's possible to override the default OVLO threshold and adjust it to an user defined value as per the system requirements. This can be achieved by dividing the input supply and feeding it to the OVLO pin. Whenever the voltage at the OVLO pin rises above a threshold $V_{OVLO(R)}$, the device turns OFF the FET. When the voltage at the OVLO pin falls below the threshold $V_{OVLO(F)}$, the FET is turned ON again. The rising and falling thresholds on this pin are slightly different, thereby providing some hysteresis and ensuring stable operation around the threshold voltage.

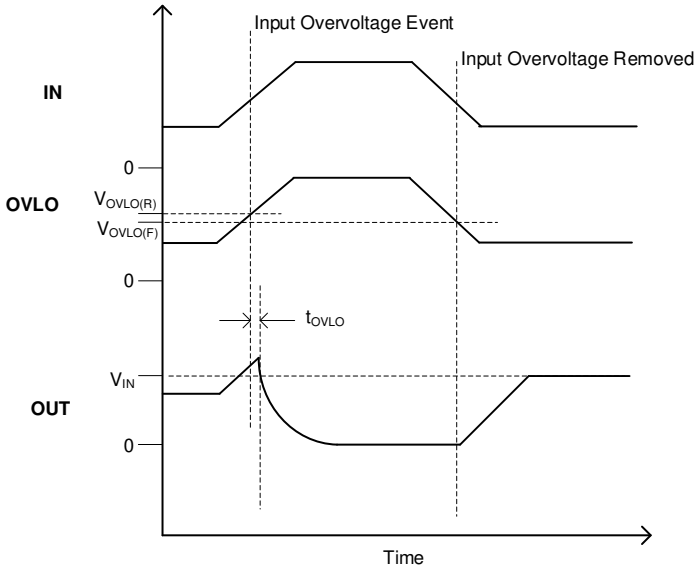


Figure 7-3. TPS25961 Adjustable Overvoltage Lockout Response

The user should choose the resistor divider values appropriately to map the desired input overvoltage level to the OVLO threshold of the part.

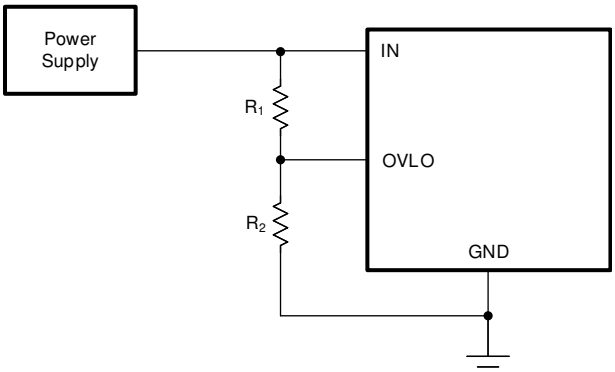


Figure 7-4. TPS25961 Adjustable Overvoltage Lockout

The equation below shows the calculations for the resistor divider values to be used to set the OVLO set-point for a given voltage supply.

$$\mathrm{VIN(OV)} = \mathrm{VOVLO(F)} \times \frac{\mathrm{R1} + \mathrm{R2}}{\mathrm{R2}} \quad (2)$$

7.3.3 Inrush Current, Overcurrent and Short Circuit Protection

The TPS25961 incorporates three levels of protection against overcurrent:

- Fixed slew rate for inrush current control (dVdt)
- Active current limiting with adjustable limit (I_{LIM}) for overcurrent protection
- Fast short-circuit response to protect against hard short-circuits

7.3.3.1 Slew Rate and Inrush Current Control (dVdt)

The inrush current during turn on is directly proportional to the load capacitance and rising slew rate.

$$\mathrm{IINRUSH} = \mathrm{COUT} \times \mathrm{SRON} \quad (3)$$

TPS25961 provides a controlled turn on at a fixed slew rate (SR_{ON}) which helps to minimize the inrush current.

7.3.3.2 Active Current Limiting

The device responds to output overcurrent conditions by actively limiting the current.

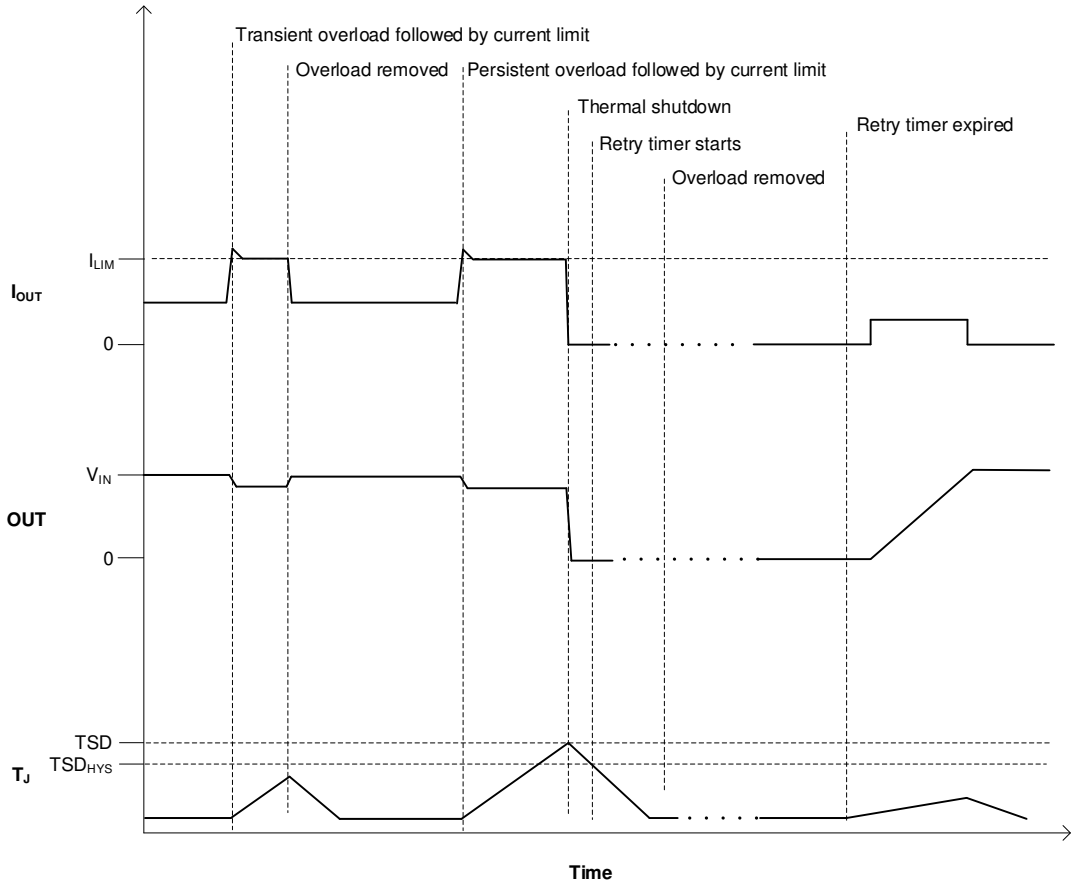


Figure 7-5. TPS25961 Overcurrent Response

In the current limiting state, the output voltage drops resulting in increased power dissipation in the internal FET leading to thermal shutdown if the condition persists for an extended period of time. In this case, the device performs 3 auto-retry attempts to allow the system to recover and then latches-off if the fault persists. See *Fault response* section for more details on device response after a fault.

The current limit threshold can be adjusted by pinstrapping the ILIM pin.

Use equation below to calculate the R_{ILIM} value for overcurrent thresholds < 200 mA.

$$\text{RILIM} = \frac{50000}{\text{ILIM - 0.000002}} \quad (4)$$

Use equation below to calculate the R_{ILIM} value for overcurrent thresholds ≥ 200 mA.

$$\text{RILIM} = \frac{50000}{\text{ILIM}} \quad (5)$$

Note

1. Leaving the ILIM pin open sets the current limit to its minimum value.
2. The device scales the FET ON resistance in discrete steps according to the R_{ILIM} setting to provide optimum performance for the desired current level. At higher I_{LIM} settings, the ON resistance is lower and at lower I_{LIM} settings, the ON resistance is higher. However, for certain R_{ILIM} resistor values, the device may select an incorrect ON resistance scaling which is too high for the target load current leading to excessive voltage drop and power dissipation. To avoid this situation, it's recommended to avoid certain R_{ILIM} values as per Table 7-1.

Table 7-1. R_{ILIM} Values to Avoid

ILIM Resistor Value	Device ON Resistance
250 kΩ < R_{ILIM} < 500 kΩ	Undefined
111 kΩ < R_{ILIM} < 142 kΩ	Undefined
58.8 kΩ < R_{ILIM} < 66.7 kΩ	Undefined

7.3.3.3 Short-Circuit Protection

The current through the device increases very rapidly during an output short-circuit event. In this event, the device engages a fast current clamping circuit to regulate down the current faster (t_{SCP}) as compared to the nominal overcurrent response time (t_{LIM}). Instead of completely turning off the power FET, the device tries to actively limit the current to ensure uninterrupted power in the event of transient overcurrents or supply transients. The device stops limiting the current once the load current falls below the programmed I_{LIM} threshold.

The output voltage drops in the current limiting state, resulting in increased power dissipation in the internal FET and might lead to thermal shutdown if the condition persists for an extended period of time. In this case, the device performs 3 auto-retry attempts to allow the system to recover and then latches-off if the fault persists. See *Fault response* section for more details on device response after a fault.

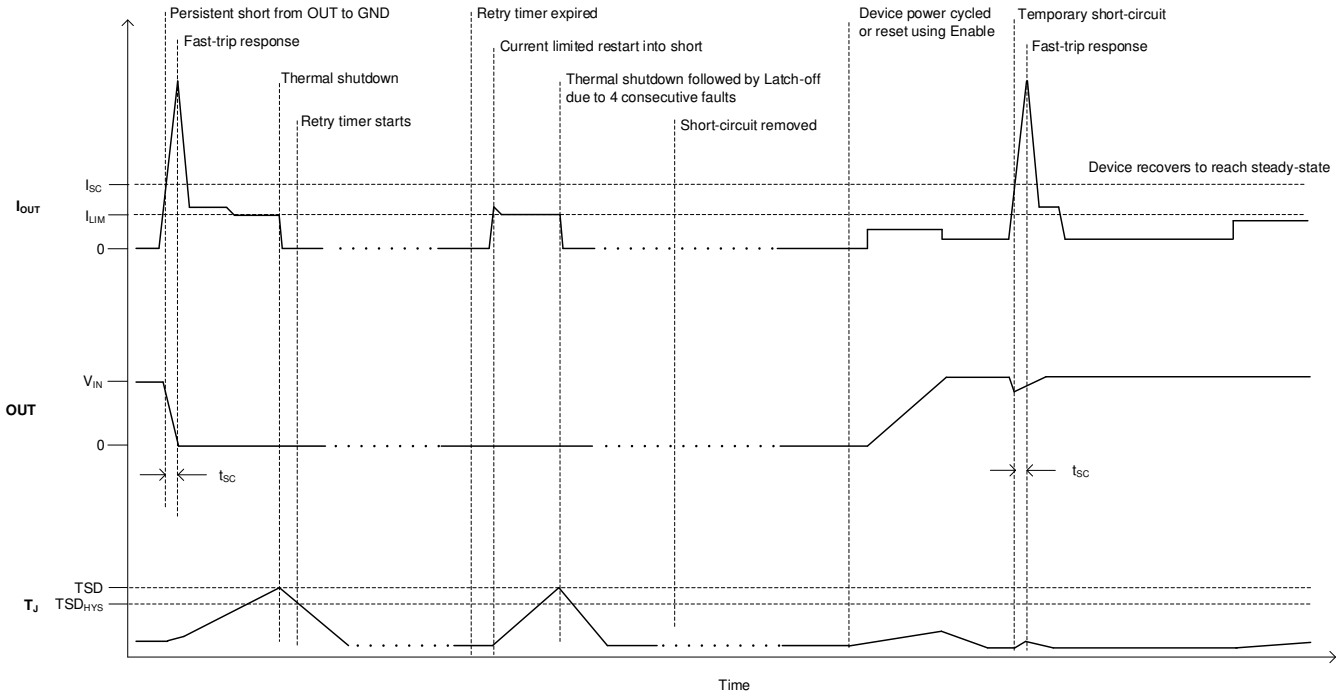


Figure 7-6. TPS25961 Short Circuit Response

7.3.4 Overtemperature Protection (OTP)

Thermal Shutdown occurs when the junction temperature (T_J) exceeds the thermal shutdown threshold (TSD). When the TPS25961 detects thermal overload, it shut downs and remains off until it has cooled down sufficiently. Once the TPS25961 junction has cooled down below TSD - TSD_{HYS}, it remains off for an additional delay of $t_{TSD,RST}$ after which it automatically retries to turn on. The device performs 3 auto-retry attempts to allow the system to recover before it latches-off if the fault persists. See *Fault response* section for more details on device response after a fault.

Table 7-2. TPS25961 Thermal Shutdown

Enter TSD	Exit TSD
$T_J \geq$ TSD	$T_J <$ TSD - TSD_{HYS} and $t_{TSD,RST}$ timer expired

7.3.5 Fault Response

Table 7-3 summarizes the protection response to various fault conditions.

Table 7-3. Fault Response

Event / Fault	Protection Response	Fault Latched Internally
Steady-state	N/A	N/A
Overtemperature	Shutdown	Yes
Undervoltage	Cut-off	No
Overvoltage	Cut-off	No
Overcurrent	Current Limit	No
Short-circuit	Current Limit	No

Once the device turns off due to a latched fault, power cycling the part or pulling the EN/UVLO pin voltage below $V_{SD(F)}$ clears the fault. Pulling the EN/UVLO just below the UVLO threshold has no impact on the device in this condition.

At the end of the $t_{TSD,RST}$ timer after a latched fault, the device will attempt to automatically restart 3 times. If the fault was caused by a transient condition which goes away and the device is able to recover and reach steady state, it clears the fault counter.

If the fault is persistent, the device will eventually shut down completely after 3 attempts and then remain latched-off till it's power cycled.

7.4 Device Functional Modes

The features of the device depend on the operating mode.

Table 7-4. Overvoltage protection modes

OVLO pin	OVLO threshold
< 0.1 V or connected to GND	Fixed 5.98 V
Resistor ladder from IN	Adjustable

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS25961 device is an integrated eFuse that is typically used for input hot-swap and power rail protection applications for systems such as energy meters, set-top boxes, building automation and adapter input protection. The device operates from 2.7-V to 19-V with adjustable current limit, overvoltage and undervoltage protection. The device aids in controlling the inrush current and provides current limiting during overload conditions.

The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool, TPS25961 Design Calculator, is available in the web product folder.

8.2 Typical Application

8.2.1 Adapter input protection for set-top boxes

TPS25961 can be used for input power protection in set-top boxes. Operating voltage is generally around 12-V and can vary from 10-V to 14-V. During event like input voltage overshoot, TPS25961 overvoltage protection acts to cut off the path and protect downstream load from overvoltage. Also inrush current control and configurable current limit feature helps in preventing power supply from collapsing during events like hotplug and overload.

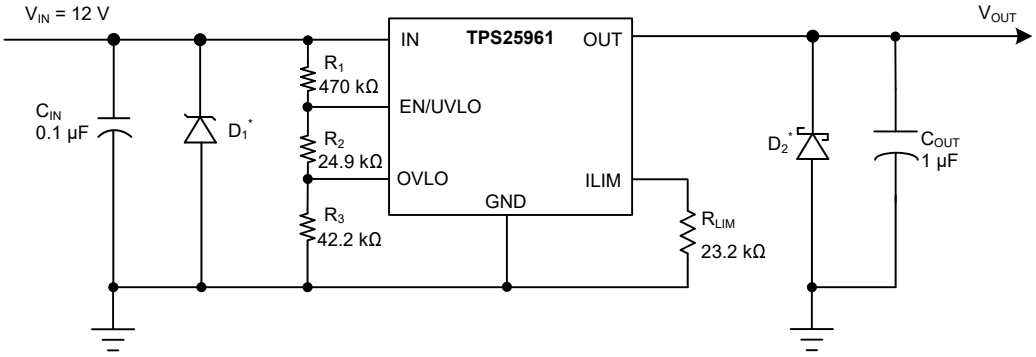


Figure 8-1. Typical Application Schematic

* Optional circuit components needed for transient protection depending on input and output inductance. Please refer to Transient Protection section for details.

8.2.2 Design Requirements

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage , V_{IN}	12 V
Undervoltage lockout set point, V_{UV}	9 V
Overvoltage protection set point , V_{OV}	15.5 V
Current limit, I_{LIM}	2 A
Load capacitance, C_{OUT}	1 µF
Maximum ambient temperature, T_A	85°C

8.2.3 Detailed Design Procedure

8.2.3.1 Programming the Current-Limit Threshold: R_{ILM} Selection

The R_{ILM} resistor at the ILM pin sets the over load current limit. Since required current limit of 2 A is greater than 200 mA, below Equation 6 for current limit can be used for calculating R_{ILIM}.

$$\text{RILIM} = \frac{50000}{\text{ILIM}} \tag{6}$$

Closest standard value resistor is 25.5 kΩ with 1% tolerance. It is recommended that final R_{ILM} selected does not lie in the ranges mentioned in Table 7-1. Final value of 25.5 kΩ does not lie in those non-recommended ranges and is fine to use in design.

8.2.3.2 Undervoltage and Overvoltage Lockout Set Point

The supply undervoltage and overvoltage thresholds are set using the resistors R1, R2 and R3 whose values can be calculated using Equation 10 and Equation 11:

$$\text{VIN(UV)} = \frac{\text{VUVLO(R)} \times (\text{R1} + \text{R2} + \text{R3})}{\text{R2} + \text{R3}} \tag{7}$$

$$\text{VIN(OV)} = \frac{\text{VOVLO(R)} \times (\text{R1} + \text{R2} + \text{R3})}{\text{R3}} \tag{8}$$

Where $V_{UVLO(R)}$ is the EN/UVLO pin rising threshold and $V_{OVLO(R)}$ is the OVLO pin rising threshold. Because R1, R2 and R3 leak the current from input supply VIN, these resistors must be selected based on the acceptable leakage current from input power supply VIN. The current drawn by R1, R2 and R3 from the power supply is IR123 = VIN / (R1 + R2 + R3). However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, IR123 must be chosen to be 20 times greater than the leakage current expected on the EN/UVLO and OVLO pins. From the device electrical specifications, both the EN/UVLO and OVLO leakage currents are 0.1 µA (maximum), $V_{OVLO(R)}$ = 1.24 V and $V_{UVLO(R)}$ = 1.24 V. From design requirements, VIN(OV) = 15.5 V and VIN(UV) = 9 V. To solve the equation, first choose the value of R1 = 470 kΩ and use the above equations to solve for R2 = 31.5 kΩ and R3 = 43.6 kΩ. Using the closest standard 1% resistor values, we get R1 = 470 kΩ, R2 = 31.6 kΩ, and R3 = 44.2 kΩ.

8.2.3.3 Output Voltage Rise Time (tR)

For a successful design, the junction temperature of device must be kept below the absolute maximum rating during both dynamic (start-up) and steady-state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to to determine that power dissipation is below a certain limit to avoid thermal shutdown during start-up.

Slew rate is 5 V/ms typically for TPS25961. The inrush current can be calculated as:

$$\text{IINRUSH (mA)} = \text{SR (V/ms)} \times \text{COUT (µF)} = 5 \times 1 = 5 \text{ mA} \tag{9}$$

The average power dissipation inside the part during inrush can be calculated as:

$$\text{PDINRUSH (W)} = \frac{\text{IINRUSH (A)} \times \text{VIN (V)}}{2} = \frac{0.005 \times 12}{2} = 0.03 \text{ W} \tag{10}$$

For the given power dissipation, the thermal shutdown time of the device must be greater than the ramp-up time t_R to avoid start-up failure. Figure 8-2 shows the thermal shutdown limit, for 0.03 W of power, the shutdown time is very large as compared to t_R = 2.4 ms. Therefore this application will have successful startup.

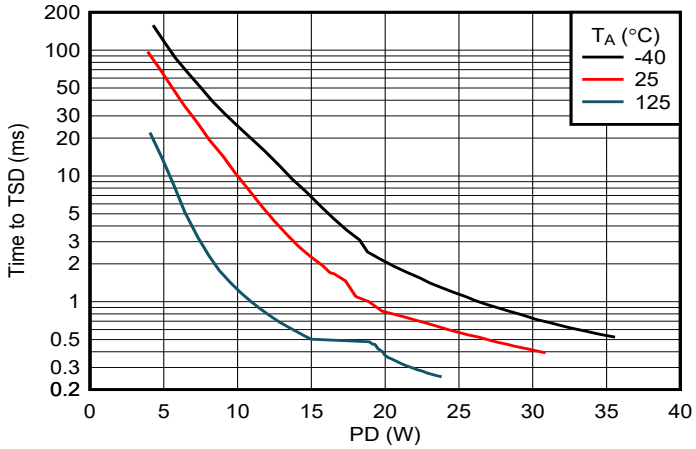


Figure 8-2. Time to Thermal Shutdown vs Power Dissipation

8.2.4 Application Curves

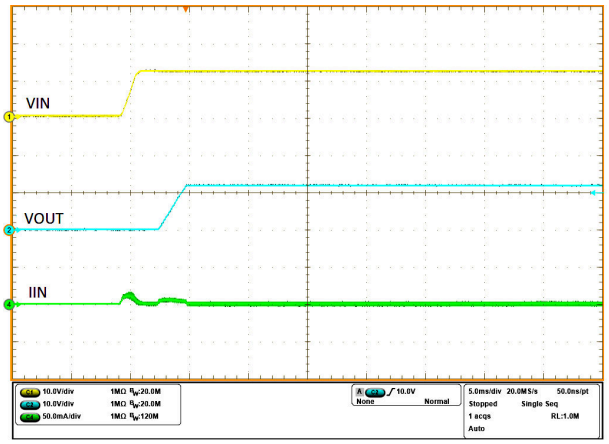


Figure 8-3. Output Ramp

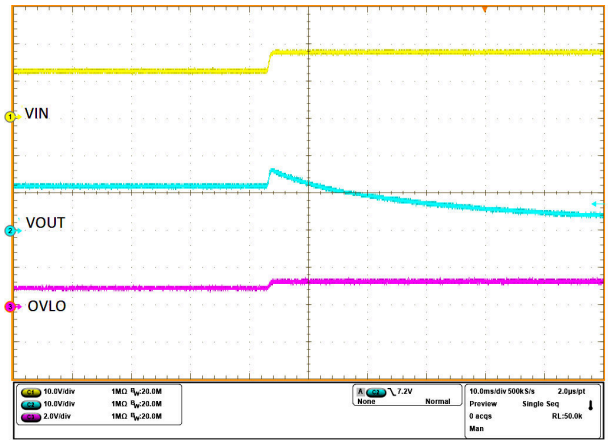


Figure 8-4. Overvoltage Protection (OVLO)

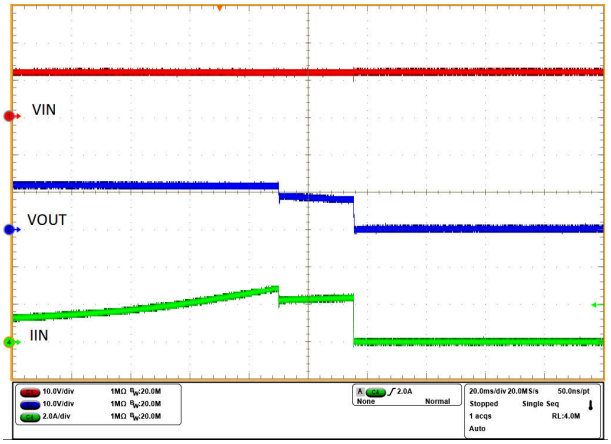


Figure 8-5. Overcurrent Protection

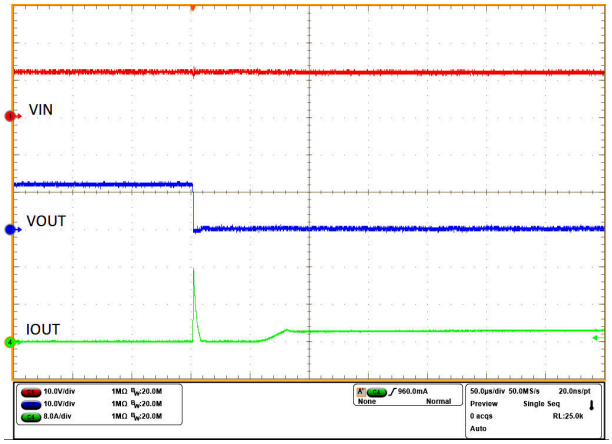


Figure 8-6. Short at Output Protection

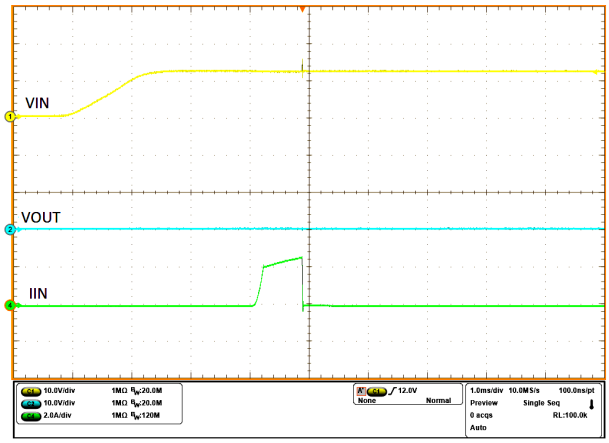


Figure 8-7. Wakeup in Short Protection

8.3 Application Example

TPS25961 can also be used as a low cost current limiter device replacing discrete PTC for memory card port protection in end equipments like IP camera, Laptop etc. Typical SD cards operate at 3.3-V and draw current less than 100 mA. TPS25961 can be configured for protection in this application without the need for many external components. Keeping OVLO pin grounded and ILIM pin open would set fixed overvoltage protection thresold of 5.98 V and current limit of 115 mA. EN pin can be tied to VIN pin through a pullup resistor. Figure 8-9 shows example layout for TPS25961 for above mentioned configuration, achieved on a single layer board with minimum components.

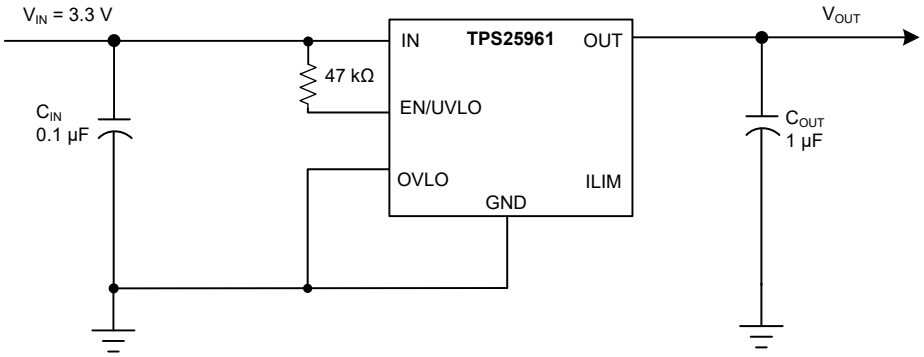


Figure 8-8. SD card port protection using TPS25961

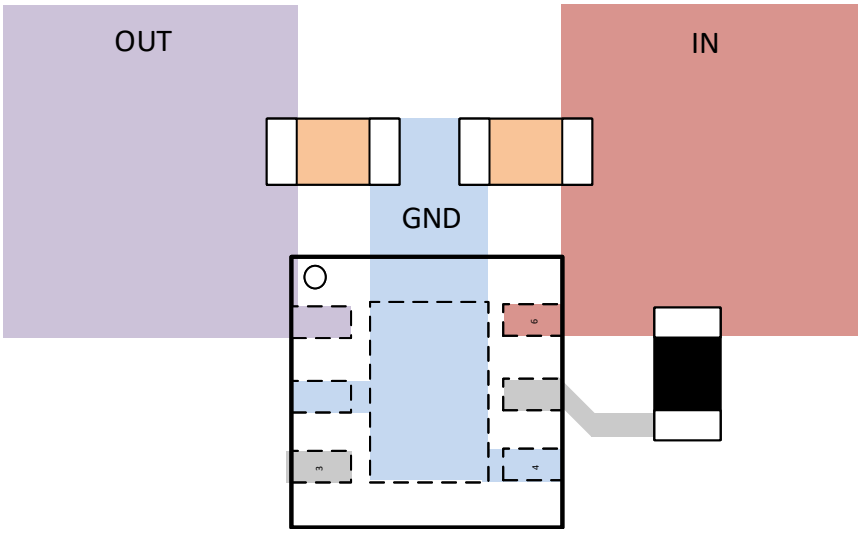


Figure 8-9. TPS25961 layout example for SD card port protection application

8.3.1 Application Curves

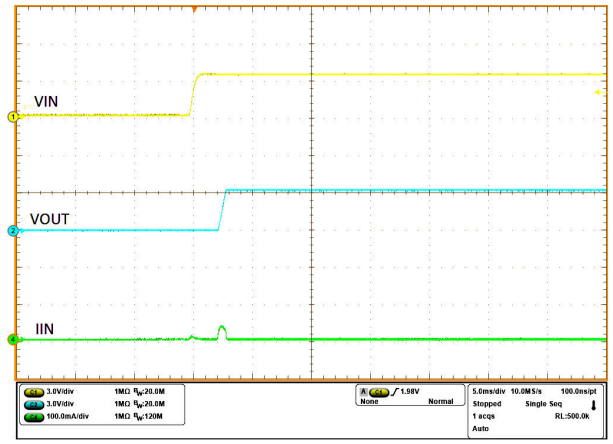


Figure 8-10. Output Ramp

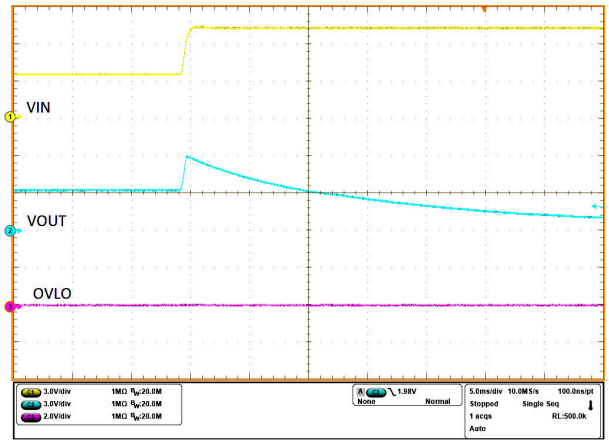


Figure 8-11. Overvoltage protection

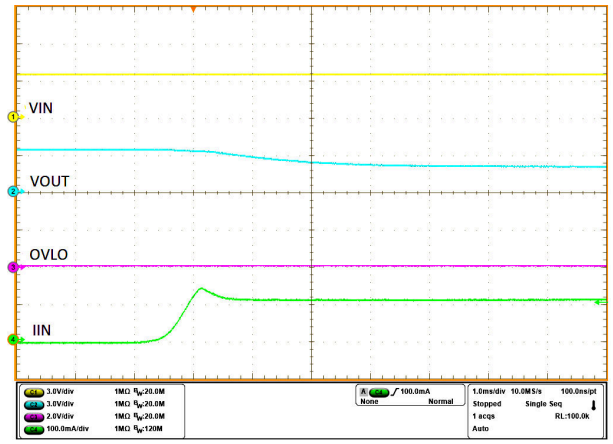


Figure 8-12. Overcurrent Protection

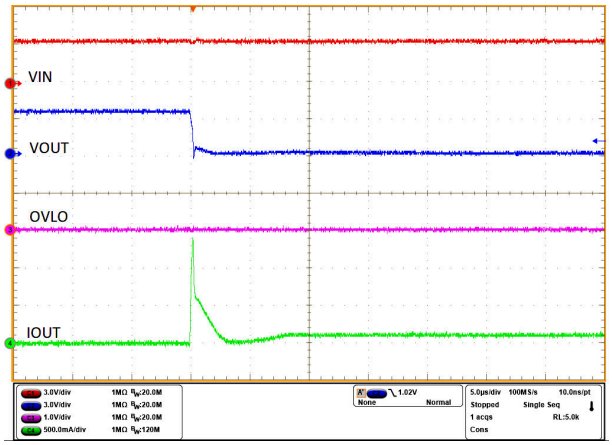


Figure 8-13. Short at Output Protection

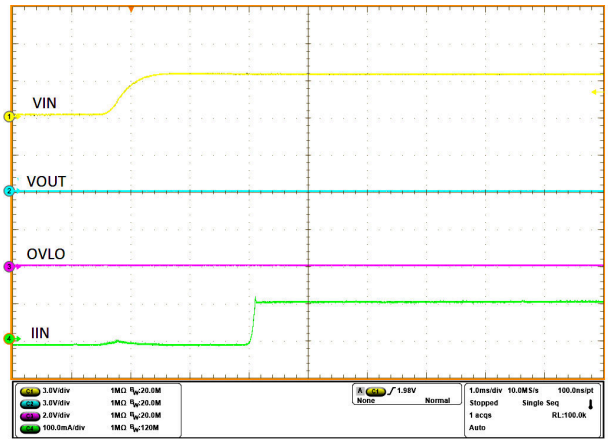


Figure 8-14. Wake up into Short Protection

8.4 Power Supply Recommendations

The TPS25961 devices are designed for a supply voltage range of 2.7-V ≤ V_{IN} ≤ 19-V. An input ceramic bypass capacitor higher than 0.1 µF is recommended if the input supply is located more than a few inches from the device. The power supply must be rated higher than the set current limit to avoid voltage droops during overcurrent and short-circuit conditions.

8.4.1 Transient Protection

In the case of a short circuit and overload current limit when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Use a Schottky diode across the output to absorb negative spikes.
- Use a low-value ceramic capacitor C_{IN} = 0.1 µF to absorb the energy and dampen the transients. The approximate value of input capacitance can be estimated using the equation below:

$$\text{VSPIKE(ABSOLUTE)} = \text{VIN} + \text{ILOAD} \times \sqrt{\frac{\text{LIN}}{\text{CIN}}} \tag{11}$$

where

- V_{IN} is the nominal supply voltage
- I_{LOAD} is the load current
- L_{IN} equals the effective inductance seen looking into the source
- C_{IN} is the capacitance present at the input

Note

NOTE: Systems which need to pass IEC 61000-4-4 tests for immunity to Electrical Fast Transients (EFT) should use a minimum C_{IN} of 2.2 µF to ensure the TPS25961 does not turn OFF during the EFT burst.

Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. The circuit implementation with optional protection components (a ceramic capacitor, TVS and Schottky diode) is shown in Figure 8-15.

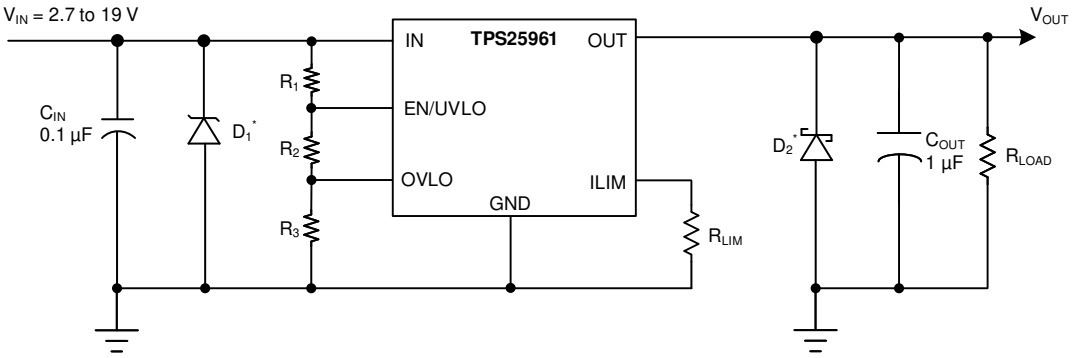


Figure 8-15. Circuit Implementation with Optional Protection Components

8.4.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

8.5 Layout

8.5.1 Layout Guidelines

- For all applications, a ceramic decoupling capacitor of 0.1 µF or greater is recommended between the IN terminal and GND terminal. For hot-plug applications, where input power-path inductance is negligible, this capacitor can be eliminated or minimized.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground must be a copper plane or island on the board.
- Locate the following support components close to their connection pins:
  - R_{ILIM}
  - Resistor network for the EN/UVLO pin
  - Resistor network for the OVLO pin

  Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing from the components to the device pins must be as short as possible to reduce parasitic effects on the current limit and overvoltage response. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT pins.
- Obtaining acceptable performance with alternate layout schemes is possible. The example shown in Section 8.5.2 has been shown to produce good results and is intended as a guideline.

8.5.2 Layout Example

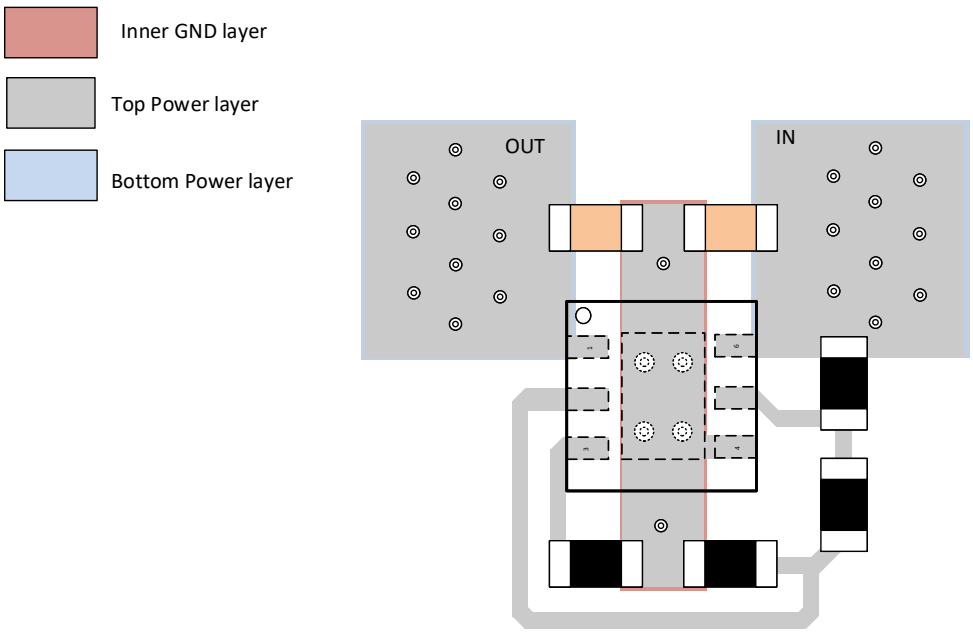


Figure 8-16. TPS25961 Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- TPS25961 Design Calculator
- TPS25961EVM eFuse Evaluation Board
- *Basics of eFuses*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS25961DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T961	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

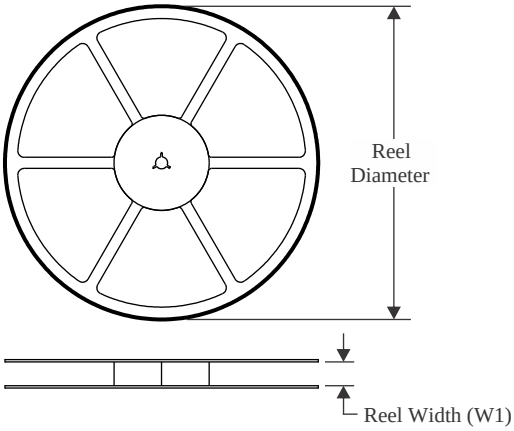
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

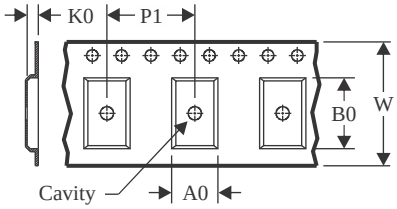
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

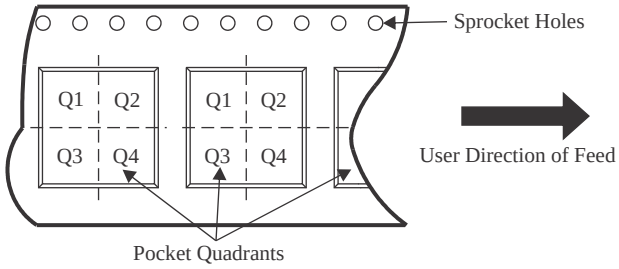


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

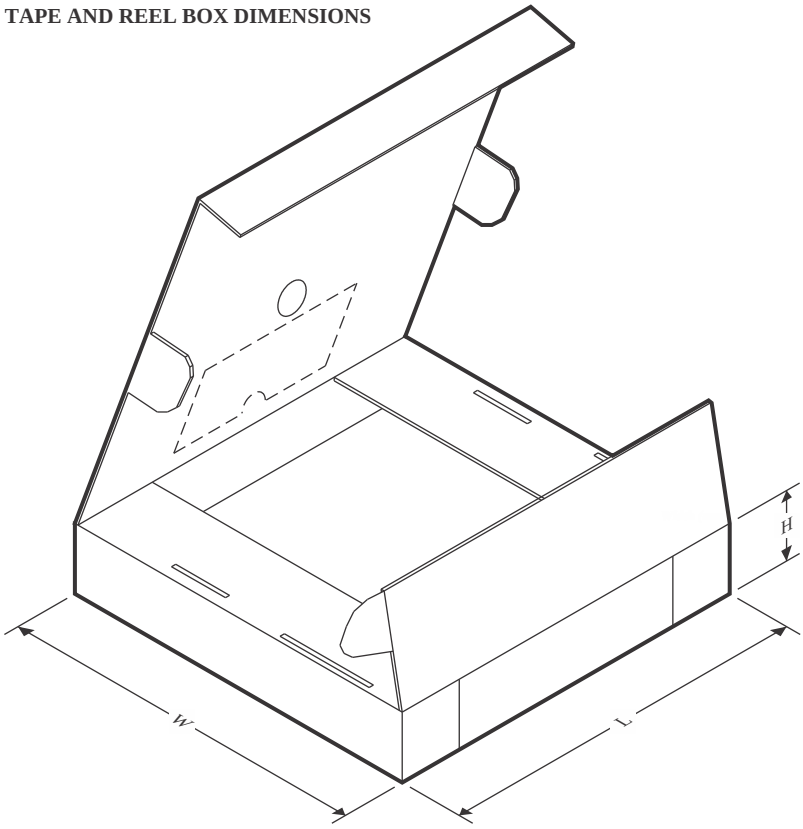
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25961DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

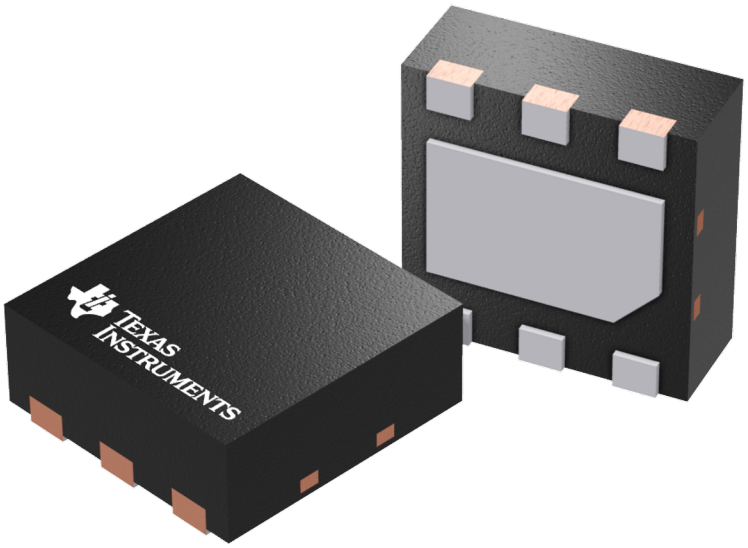


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25961DRVR	WSON	DRV	6	3000	210.0	185.0	35.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



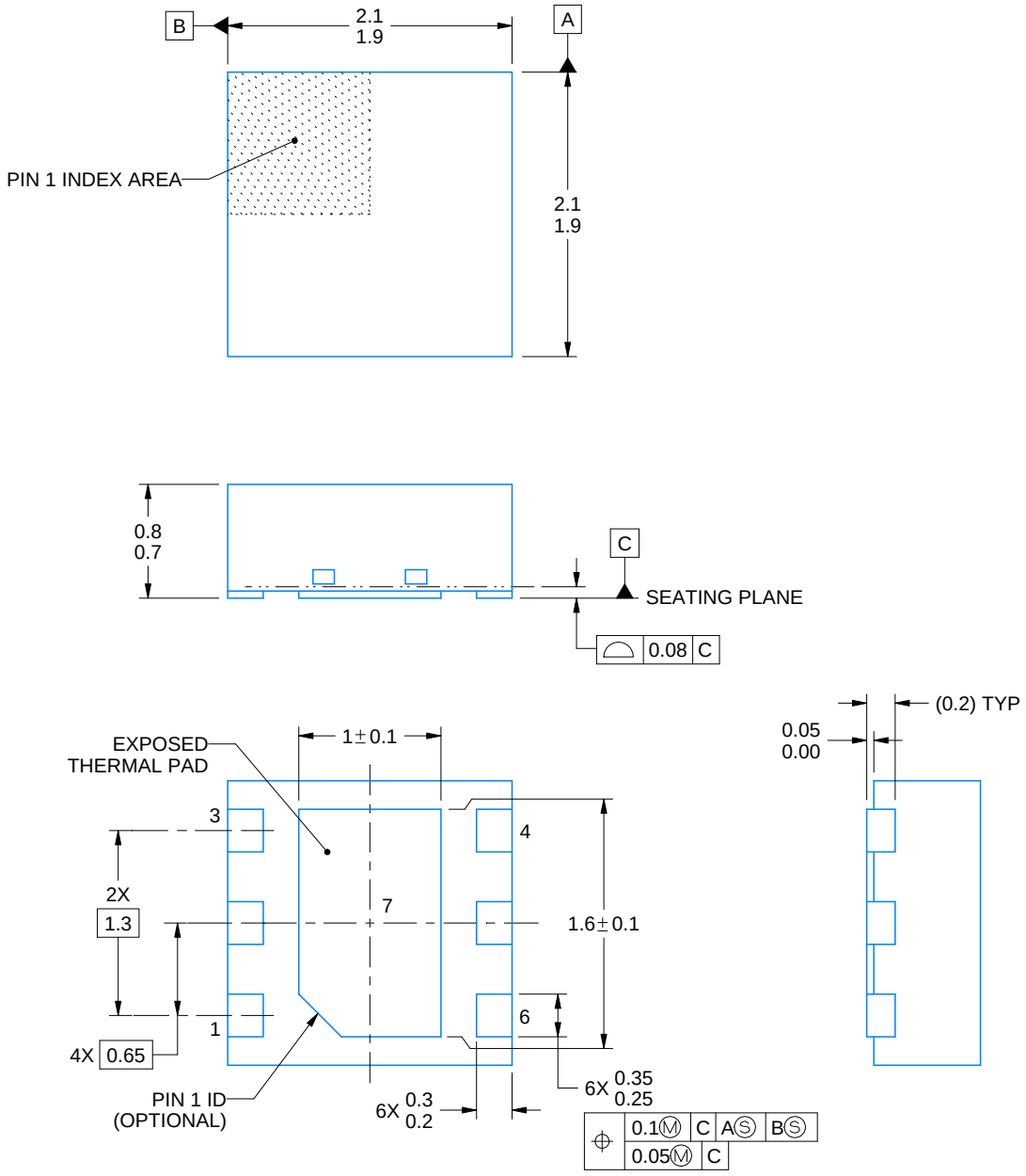
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

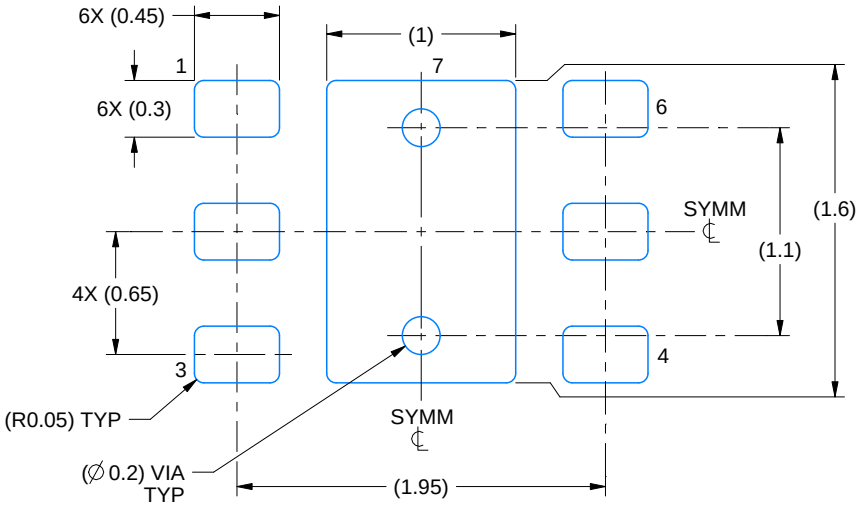
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

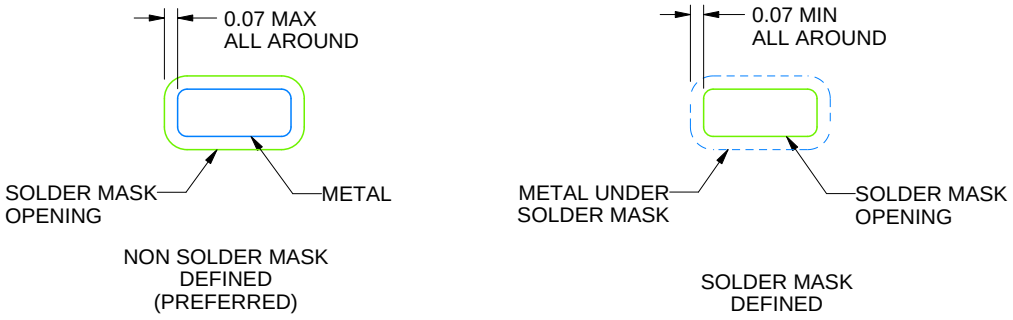


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

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NOTES: (continued)

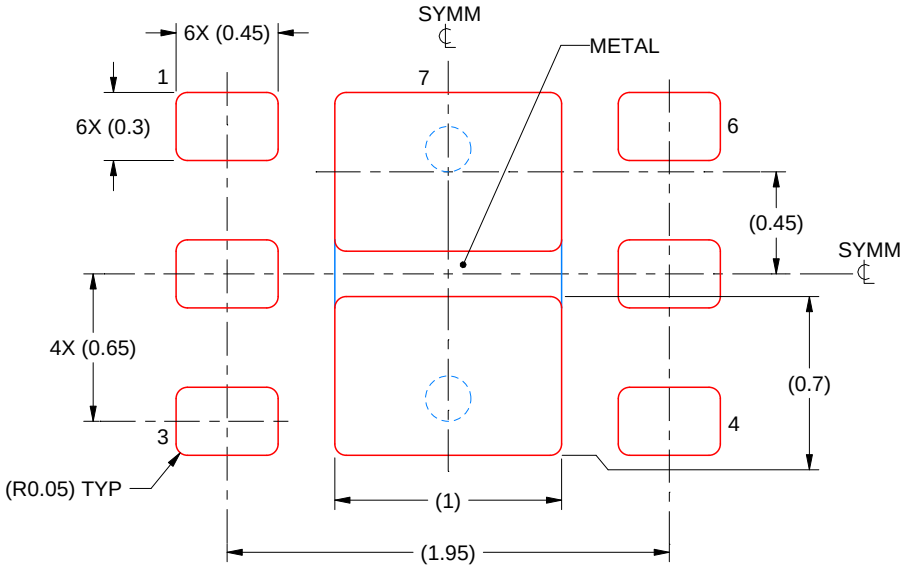
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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